

MODEL NAME : **RANGER 17**

PCB NO : **LA-9331P**

BOM P/N : **4619KL31L01**

# Compal Confidential

## RANGER 17

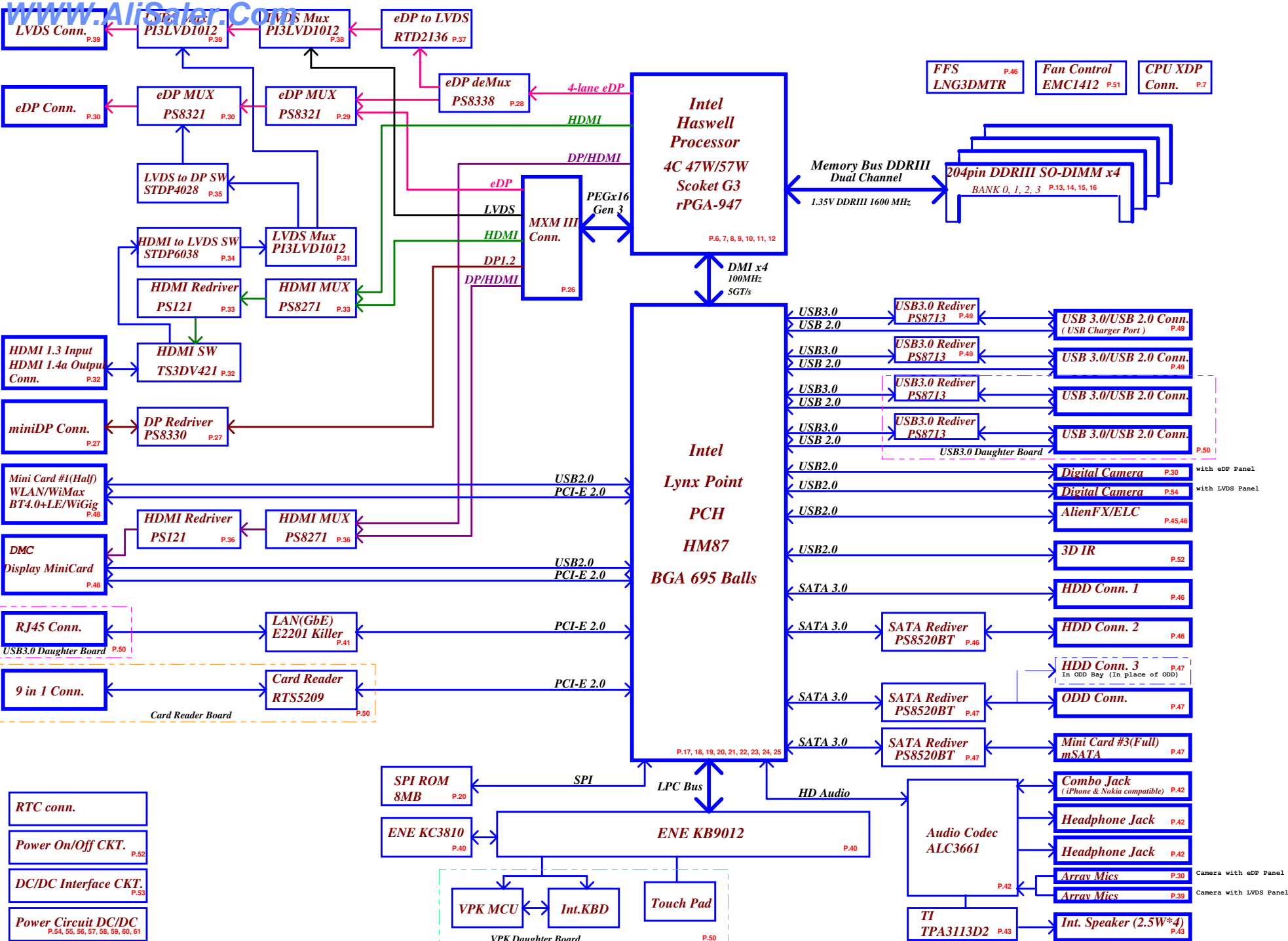
### Schematic Document

Rev: X00

2012-06-22

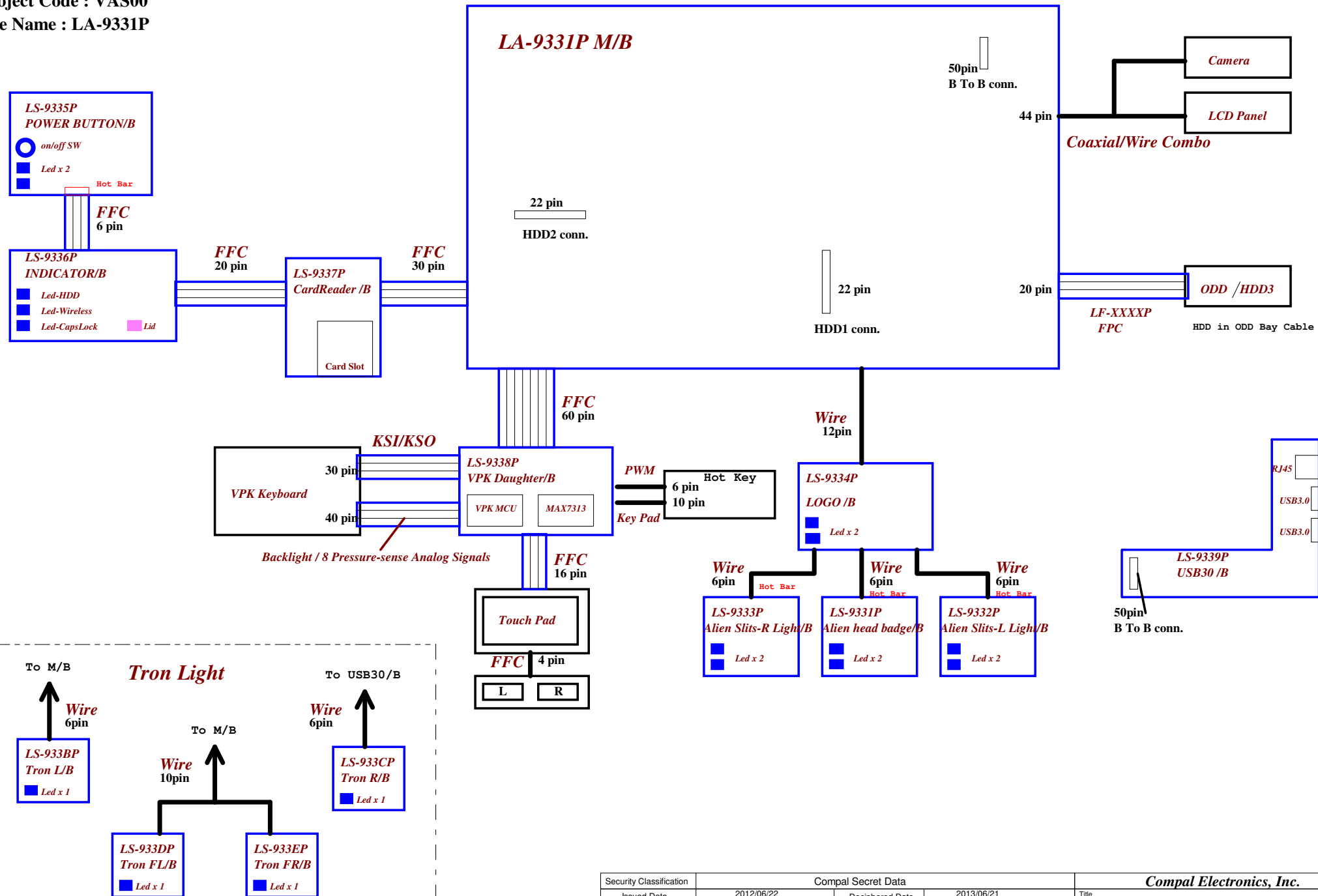
@ : Nopop Component

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Project Code : VAS00  
File Name : LA-9331P



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Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1 (SSI)
1	0.2 (PT)
2	0.3 (ST)
3	0.4 (QT)
4	1.0 (MP)
5	
6	
7	

USB 3.0 PORT	Connction
1	JUSB1 (Left side)
2	JUSB2 (Left side)
3	NA
4	NA
5	JUSB3 (Right side)
6	JUSB4 (Right side)

POWER STATES

State	Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0		HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M-OFF		LOW	HIGH		HIGH	LOW	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF		LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF		LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PM TABLE

State	power plane	+5VALW +3VALW +3VLP +3V_PCH	+1.35V +1.05V	+5VS +3VS +1.5VS +1.05VS +0.675VS +3VMXM +5VMXM +VCC_CORE +1.35V_CPU_VDDQ
S0		ON	ON	ON
S3		ON	ON	OFF
S5 S4/AC		ON	OFF	OFF
S5 S4/AC don't exist		OFF	OFF	OFF

Symbol Note :



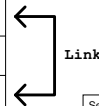
CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	MINI CARD-1 WLAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	MINI CARD-2 DMC	CLKOUTFLEX1	None
	CLKOUT_PCIE2	10/100/1G LAN	CLKOUTFLEX2	None
	CLKOUT_PCIE3	CARD READER	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_A	MXM		

SATAIII	DESTINATION
SATA0	HDD1
SATA1	HDD2
SATA2	ODD
SATA3	mSATA
SATA4/PCIE LANE1	MINI CARD-1 WLAN
SATA5/PCIE LANE2	MINI CARD-2 DMC

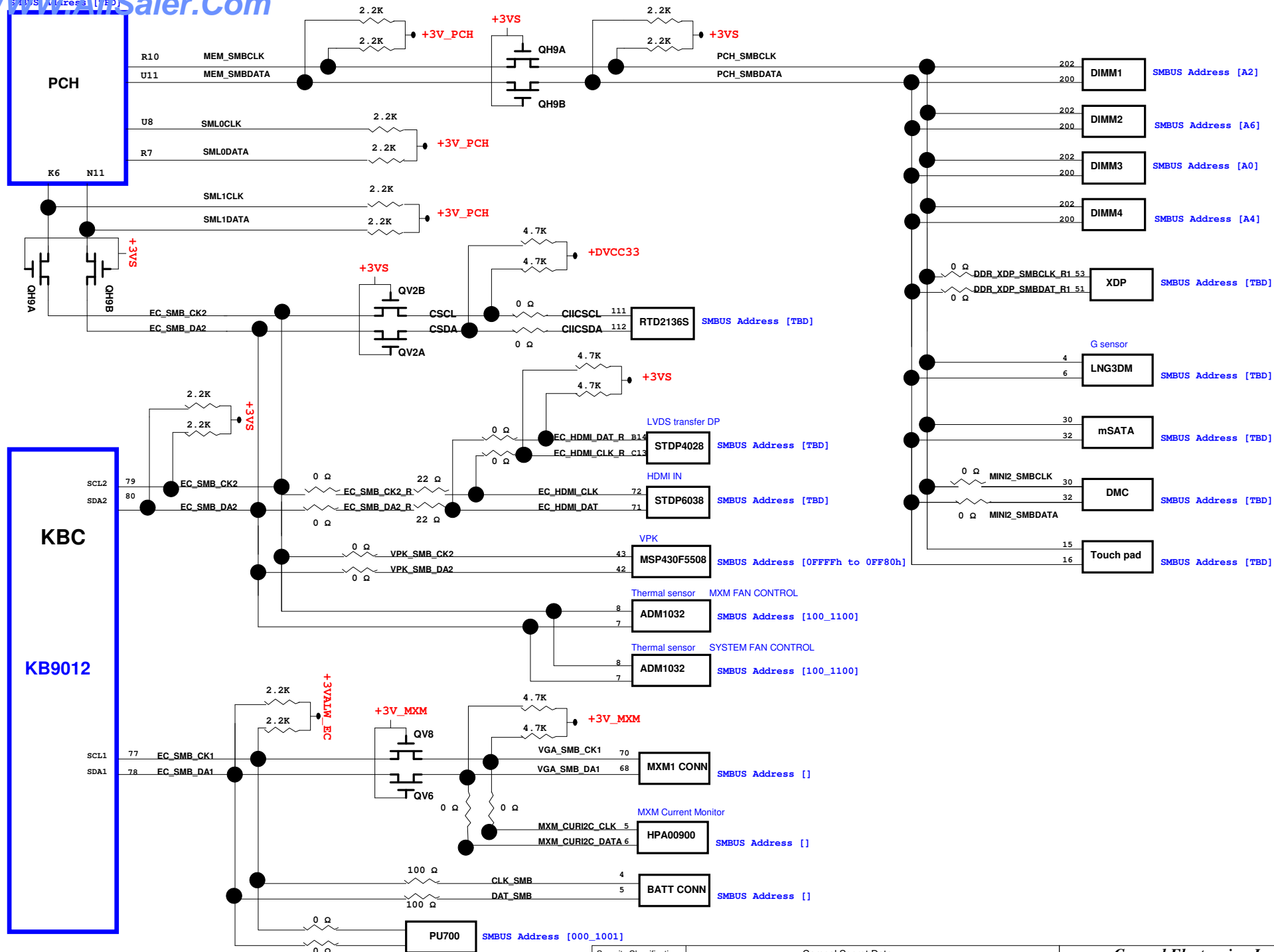
PCI EXPRESS	DESTINATION
Lane 1/USB3.0 Port 3	None
Lane 2/USB3.0 Port 4	None
Lane 3	10/100/1G LAN
Lane 4	CARD READER
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

SMBUS Control Table

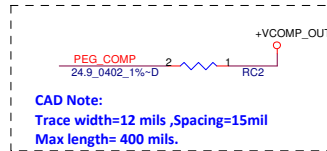
	SOURCE	WLAN	DMC	BATT	DIMM	6038	4028	Thermal Sensor	FFS	2136	VPK MCU	MXM	XDP	Charger	TP	mSATA
EC_SMB_CK1 EC_SMB_DA1	KB9012			V								V		V		
EC_SMB_CK2 EC_SMB_DA2	KB9012					V	V	V		V	V					
PCH_SMLCLK PCH_SML0DATA	PCH															
PCH_SML1CLK PCH_SML1DATA	PCH															
MEM_SMBCLK MEM_SMBDATA	PCH		V		V				V				V		V	V



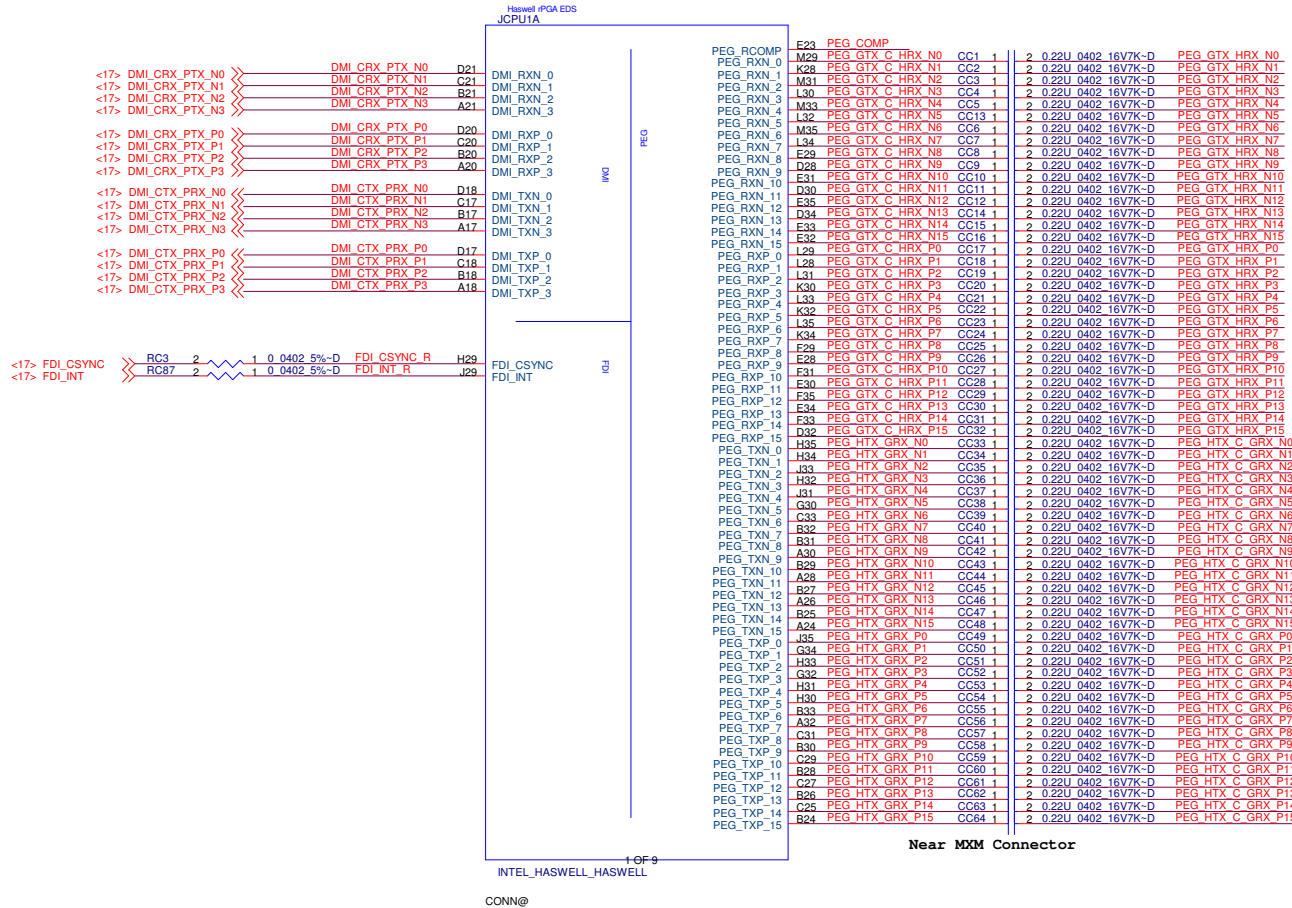
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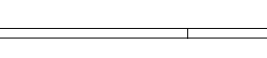
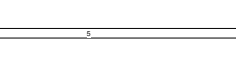
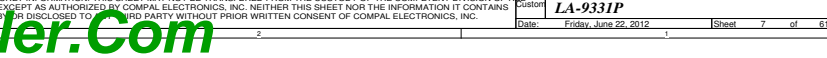
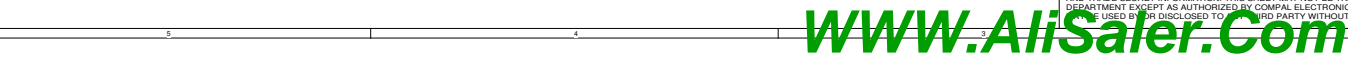
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PEG\_GTX\_HRX\_N0..15] <29>  
PEG\_HTX\_C\_GRX\_P0..15] <29>  
PEG\_HTX\_C\_GRX\_N0..15] <29>



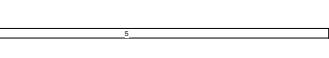
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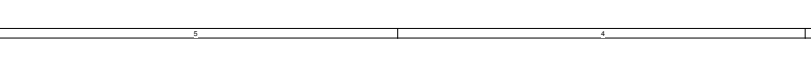


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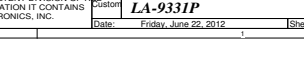
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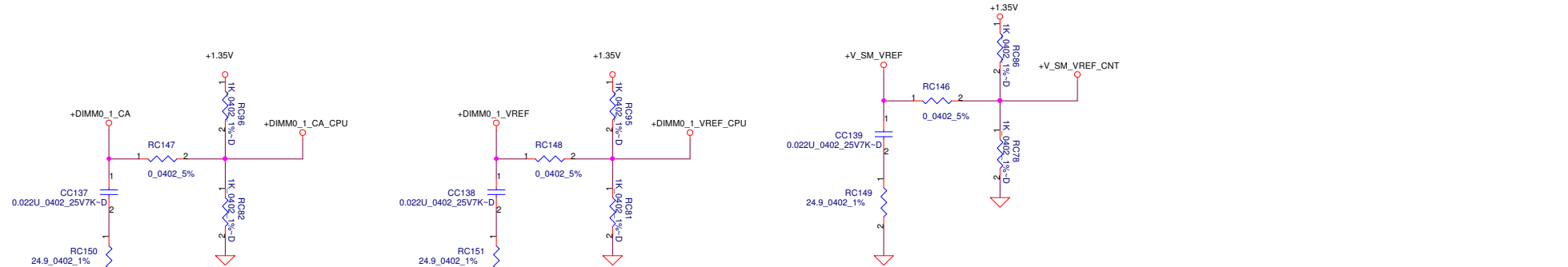
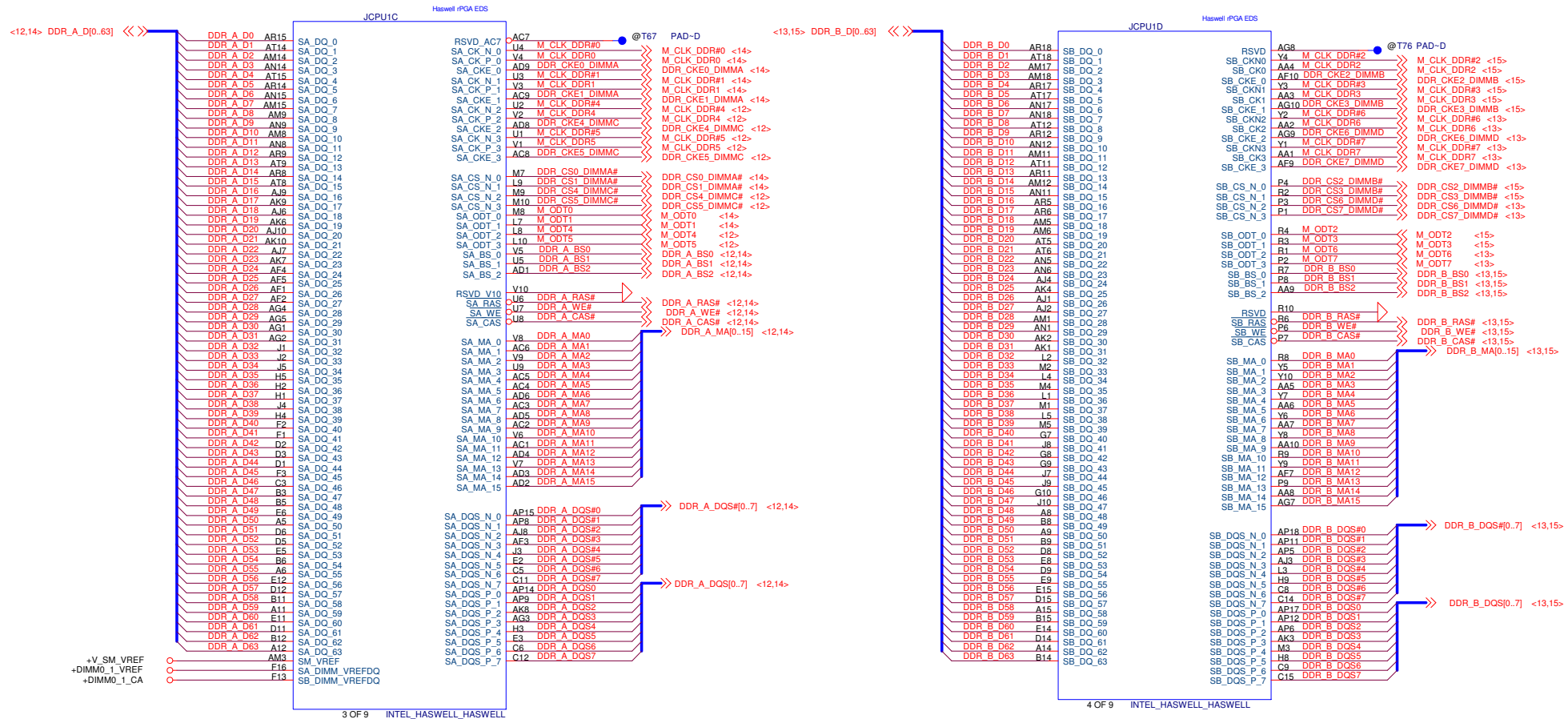


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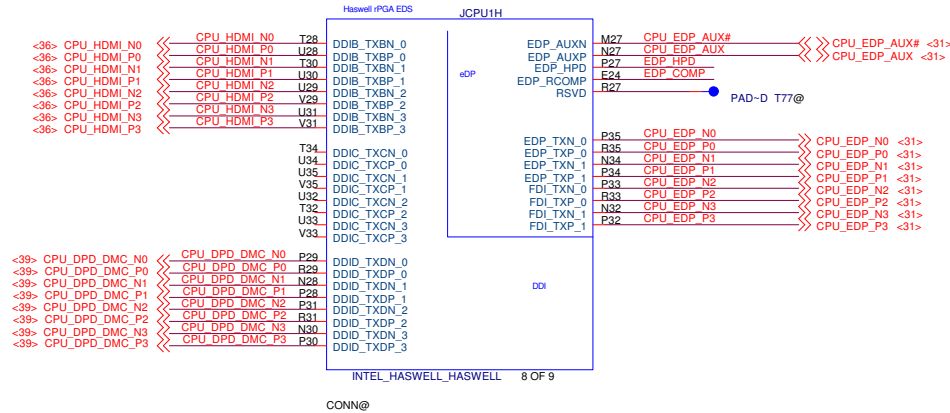
### COMPENSATION PU FOR eDP



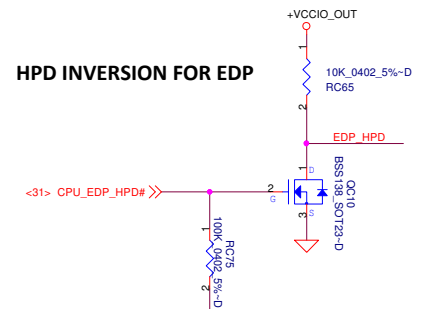
CAD Note:Trace width=20 mils ,Spacing=25mil,  
Max length=100 mils.

HDMI

DMC

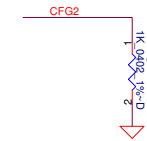


### HPD INVERSION FOR EDP

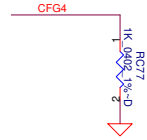


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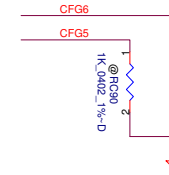
# CFG STRAPS for CPU



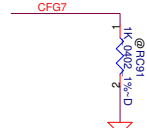
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



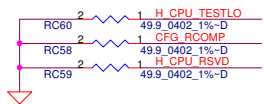
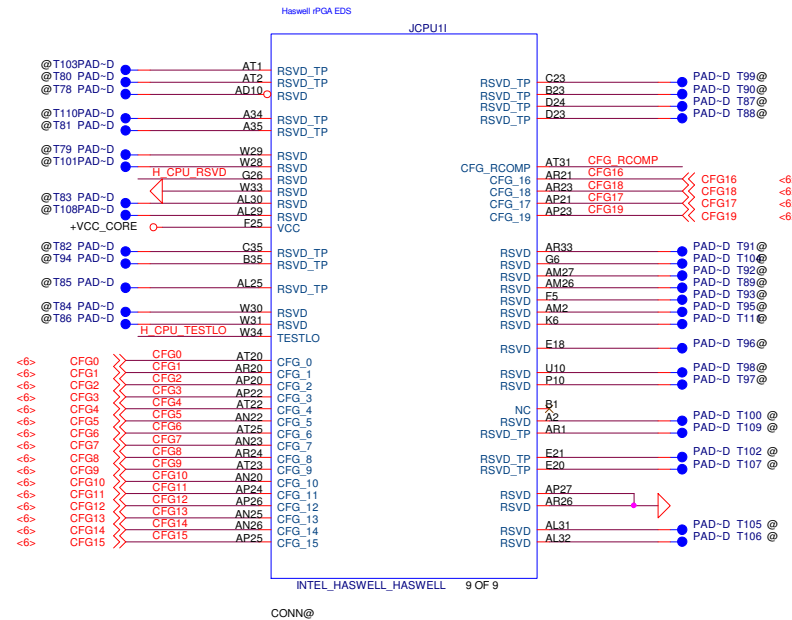
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

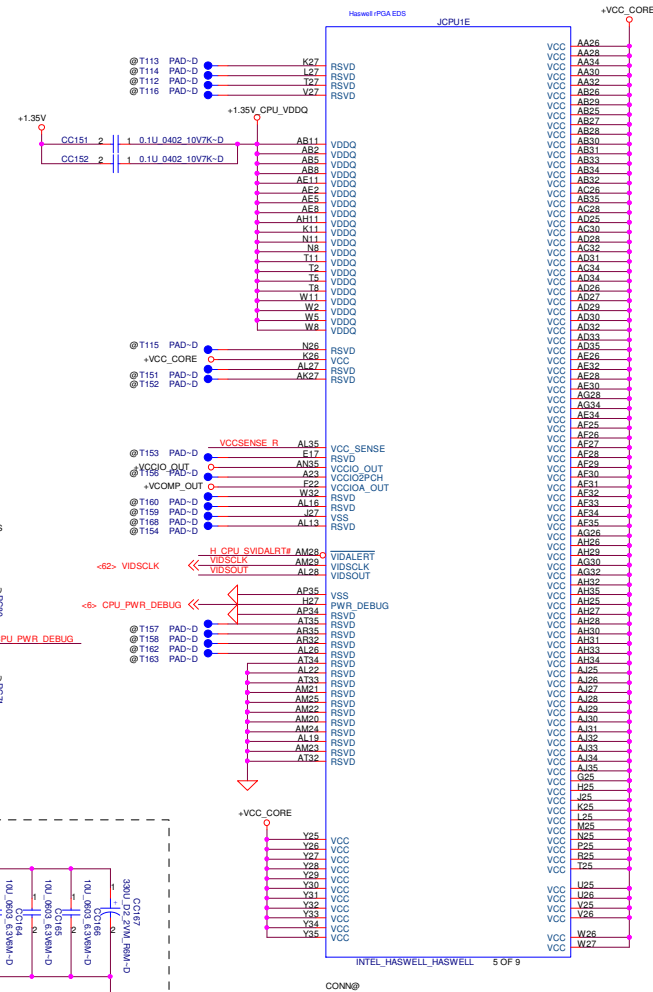
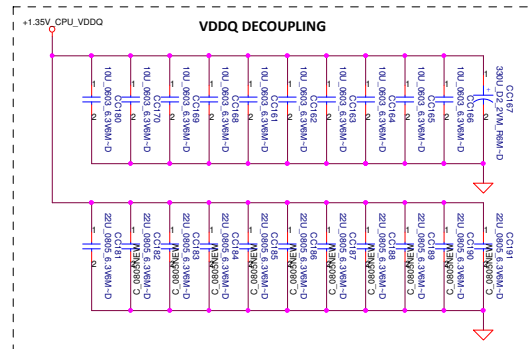
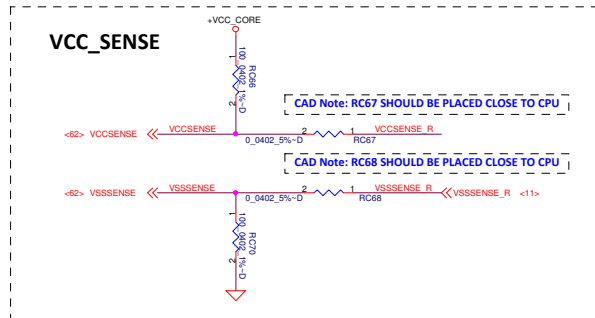


PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

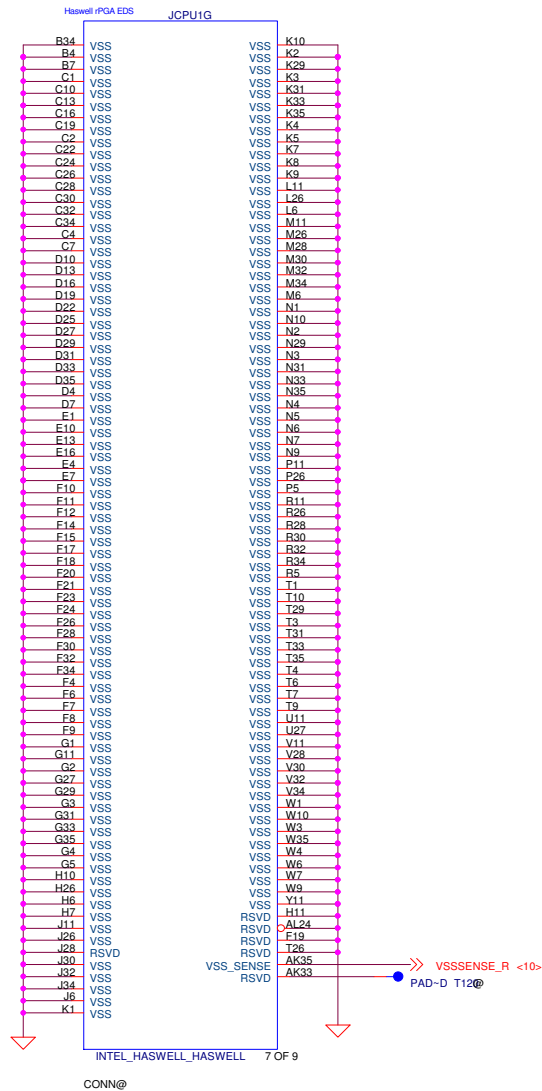
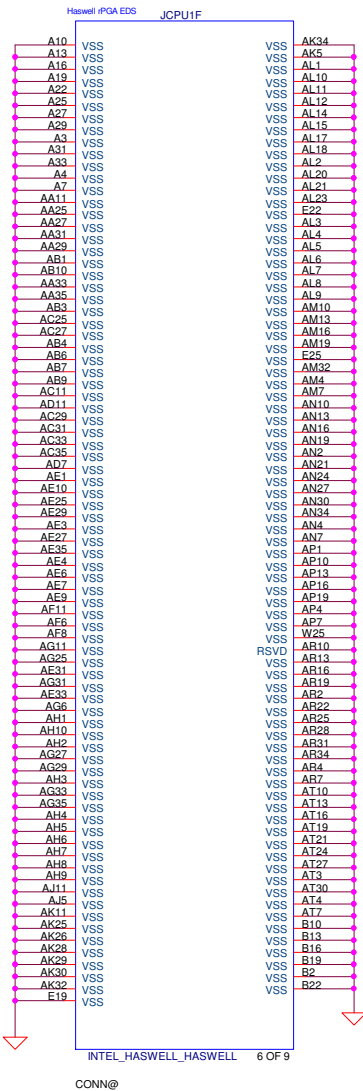


PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training





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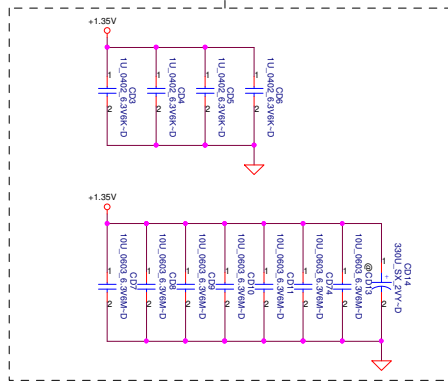


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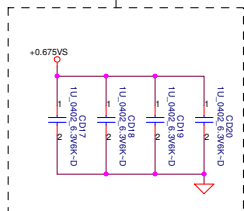
# JDIMMA H=4mm

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 <7,14> DDR\_A\_DQ[0..63] <<>  
 <7,14> DDR\_A\_DQS[0..7] <<>  
 <7,14> DDR\_A\_MA[0..15] <<>

Layout Note:  
Place near JDIMMA

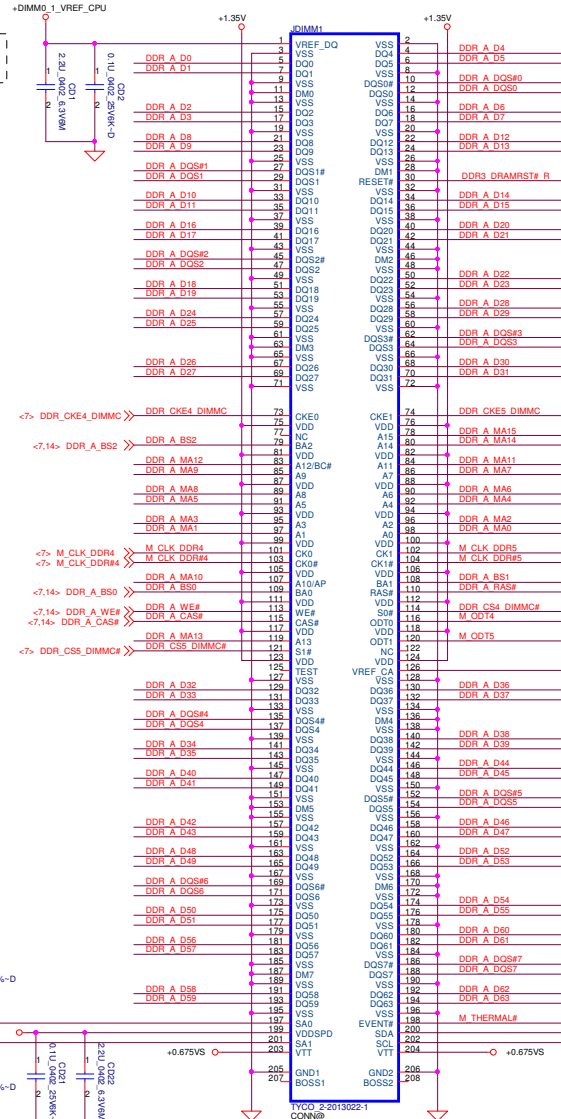


Layout Note:  
Place near JDIMMA.203,204



SA0	SA1	
1	0	DIMMIA
1	1	DIMMB
0	0	DIMMC
0	1	DIMMD

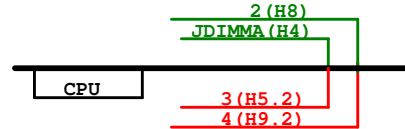
All VREF traces should have 20 mil trace width



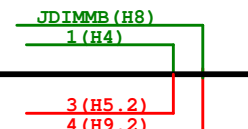
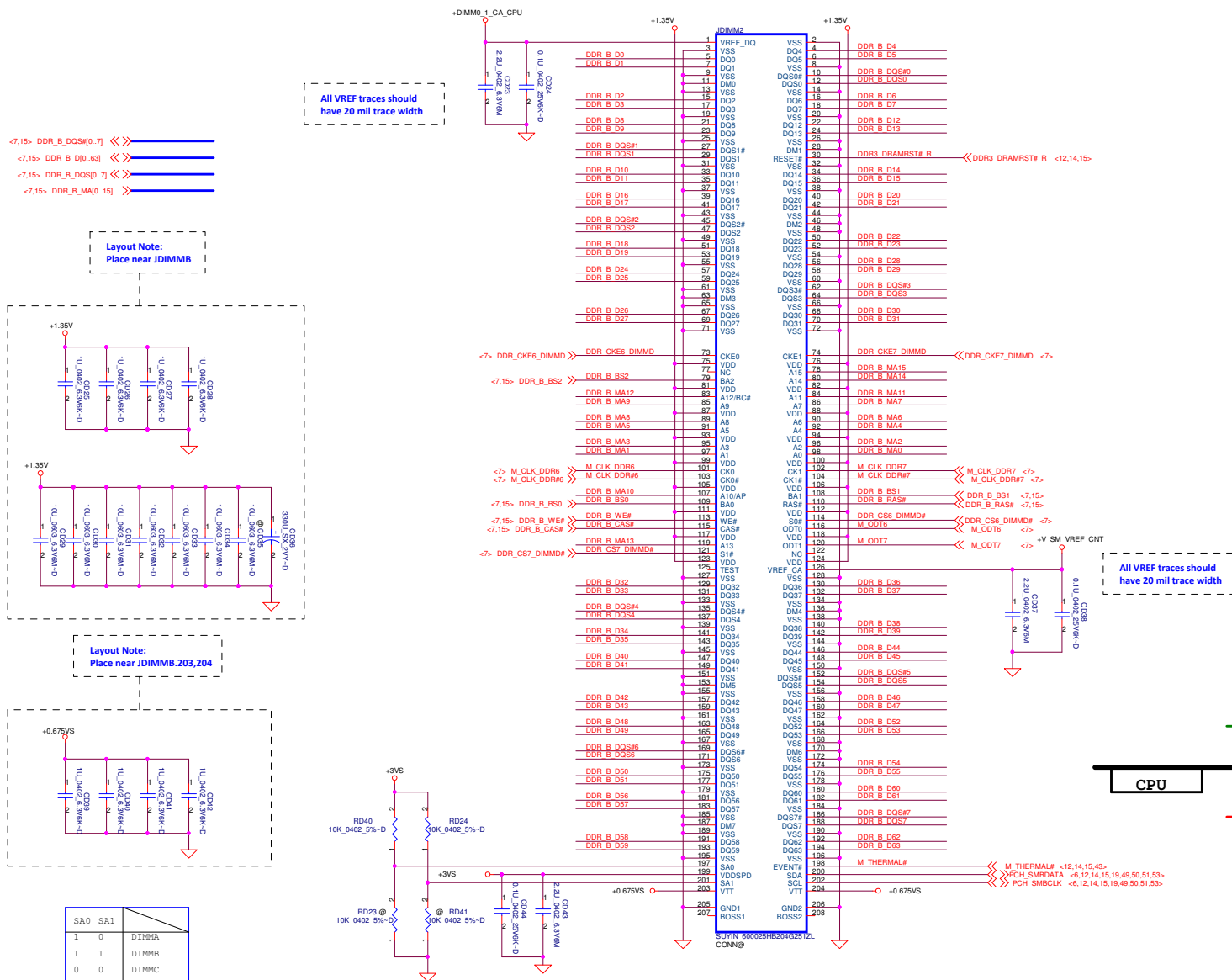
<13,14,15> DDR3\_DRAMRST#\_R <<> DDR3\_DRAMRST#\_CPU <<>

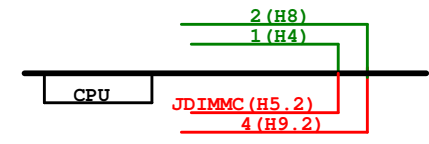


All VREF traces should have 20 mil trace width



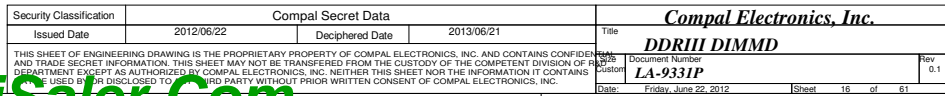
# JDIMMB H=4mm

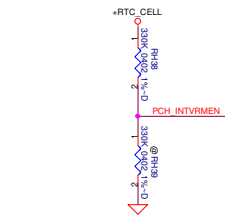




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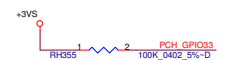


INTVRMEN - INTEGRATED SUS 1.05V VRM  
 ENABLE  
 High - Enable Internal VRs  
 Low - Enable External VRs



NO REBOOT STRAP  
 DISABLED WHEN LOW (DEFAULT)  
 ENABLED WHEN HIGH

FLASH DESCRIPTOR SECURITY OVERRIDE  
 LOW = DESABLED (DEFAULT)  
 HIGH = ENABLED

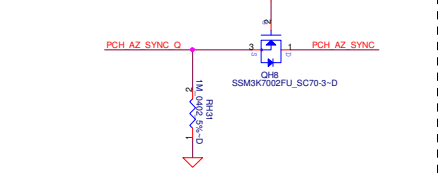


CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

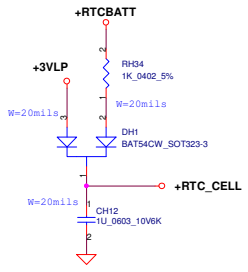
  

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

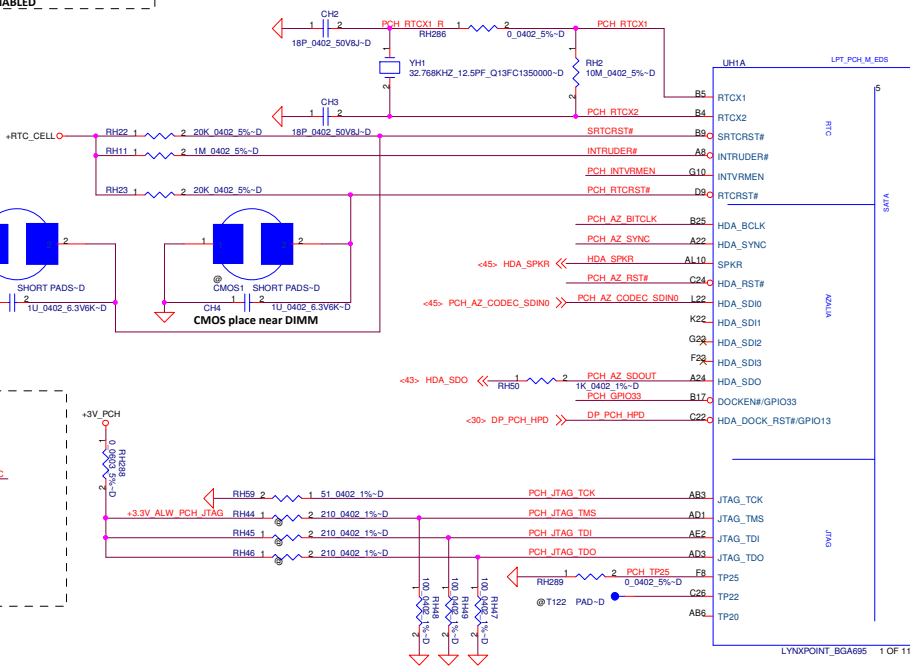
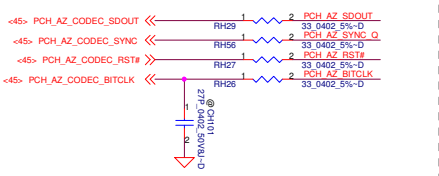
### HDA\_SYNC Isolation Circuit



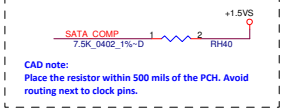
### RTC Battery

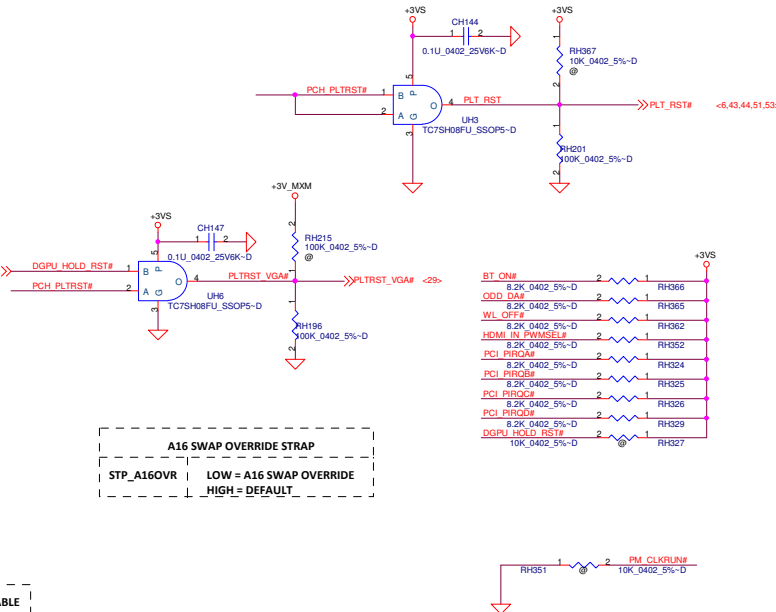
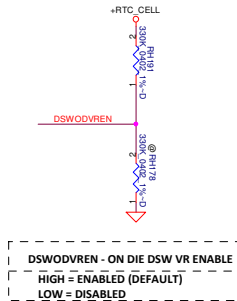


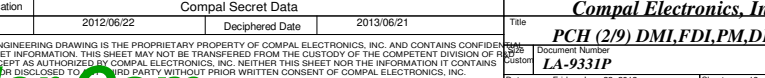
### HDA for Codec

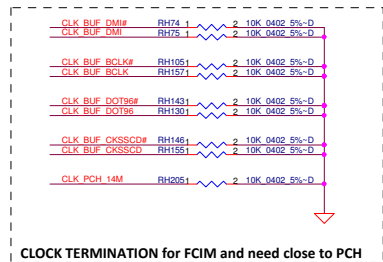


### SATA Impedance Compensation

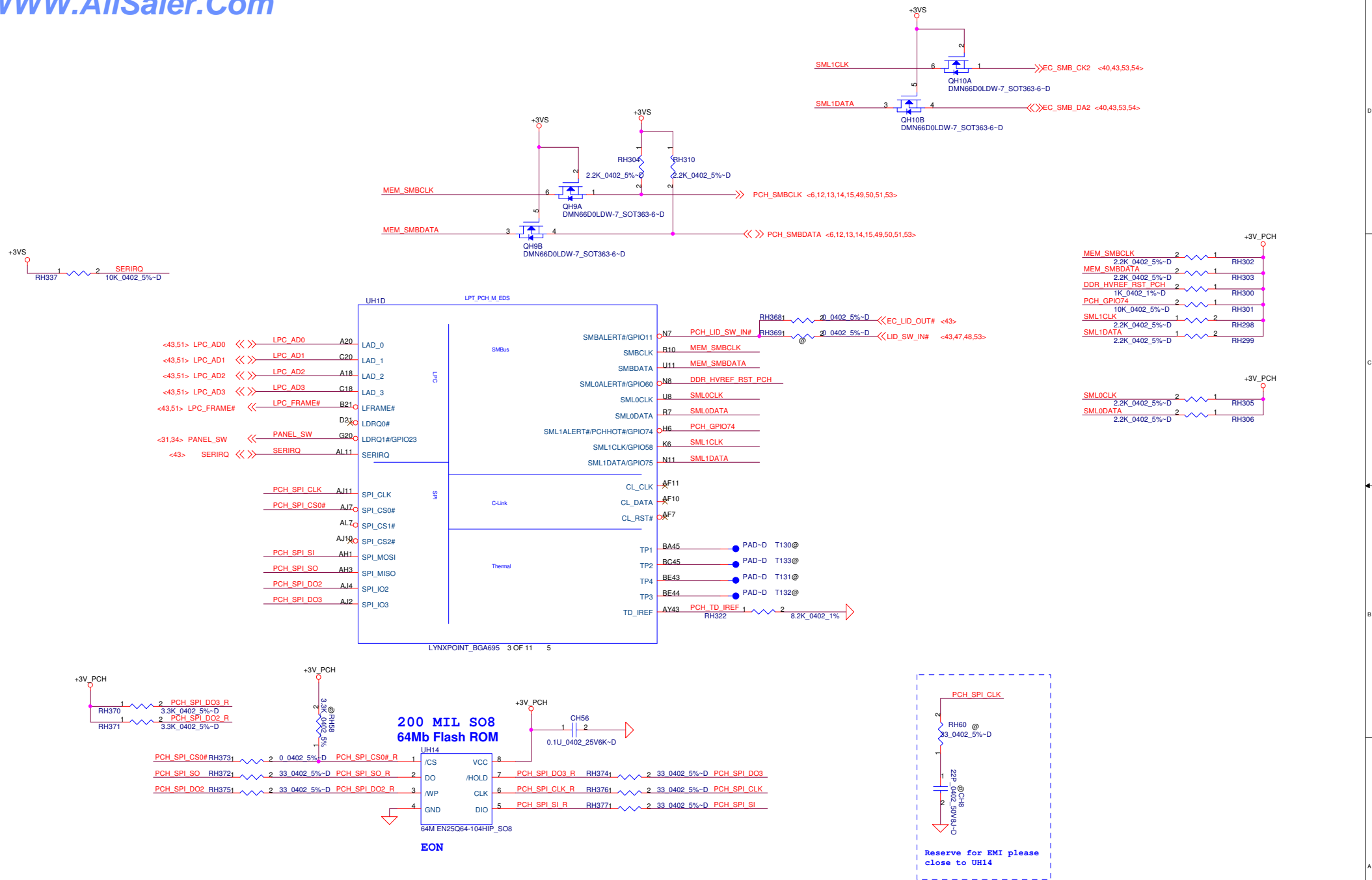




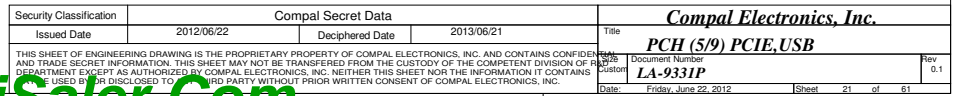
Security Classification	Compal Secret Data			Title		
Issued Date	2012/06/22	Deciphered Date	2013/06/21	PCH (2/9) DMI,FDI,PM,DP,CRT		
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				Doc. Control	14-9331P	
				Date	Friday, June 22, 2012	Sheet 18 of 61

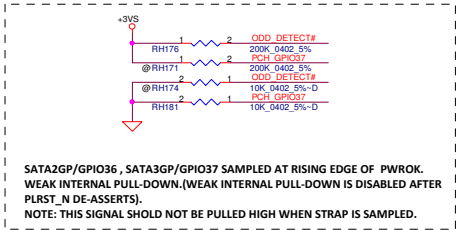


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			Date	Sheet
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Security Classification	Compal Secret Data			Title	
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				LA-9331P	0.1
				Date: Friday, June 22, 2012	Sheet 20 of 61

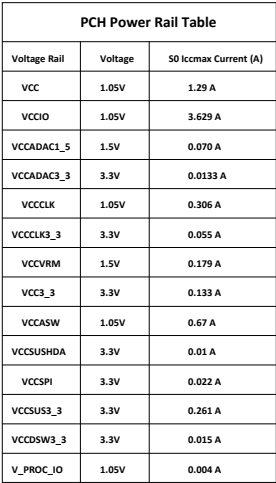




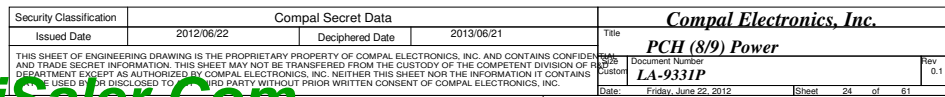
Fixed Signals				Muxed Signals		Fixed Signals						Muxed Signals		Fixed Signals			
USB3_1	USB3_2	USB3_3	USB3_6	PCIE_1	PCIE_2	PCIE_3	PCIE_4	PCIE_5	PCIE_6	PCIE_7	PCIE_8	SATA_4	SATA_5	SATA_0	SATA_1	SATA_2	SATA_3
				(00)	(00)							(00)	(00)				
				USB3_3	USB3_4							PCIE_1	PCIE_2				

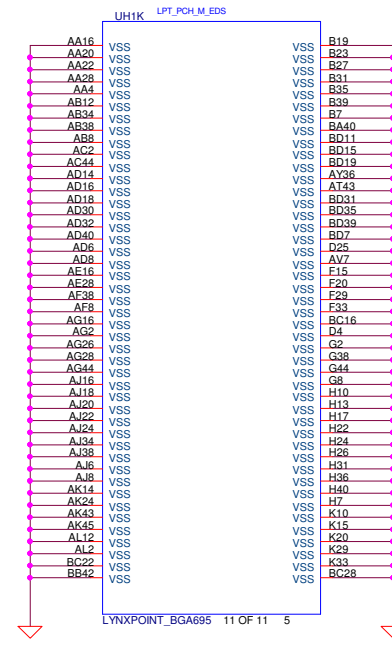
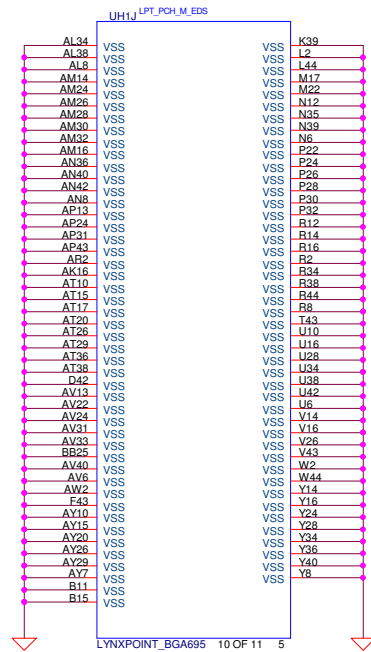
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Issued Date	2012/06/22	Deciphered Date	2013/06/21	Doc Number
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Date			LA-9331P	Rev 0.1
Date			Friday, June 22, 2012	Sheet 22 of 61

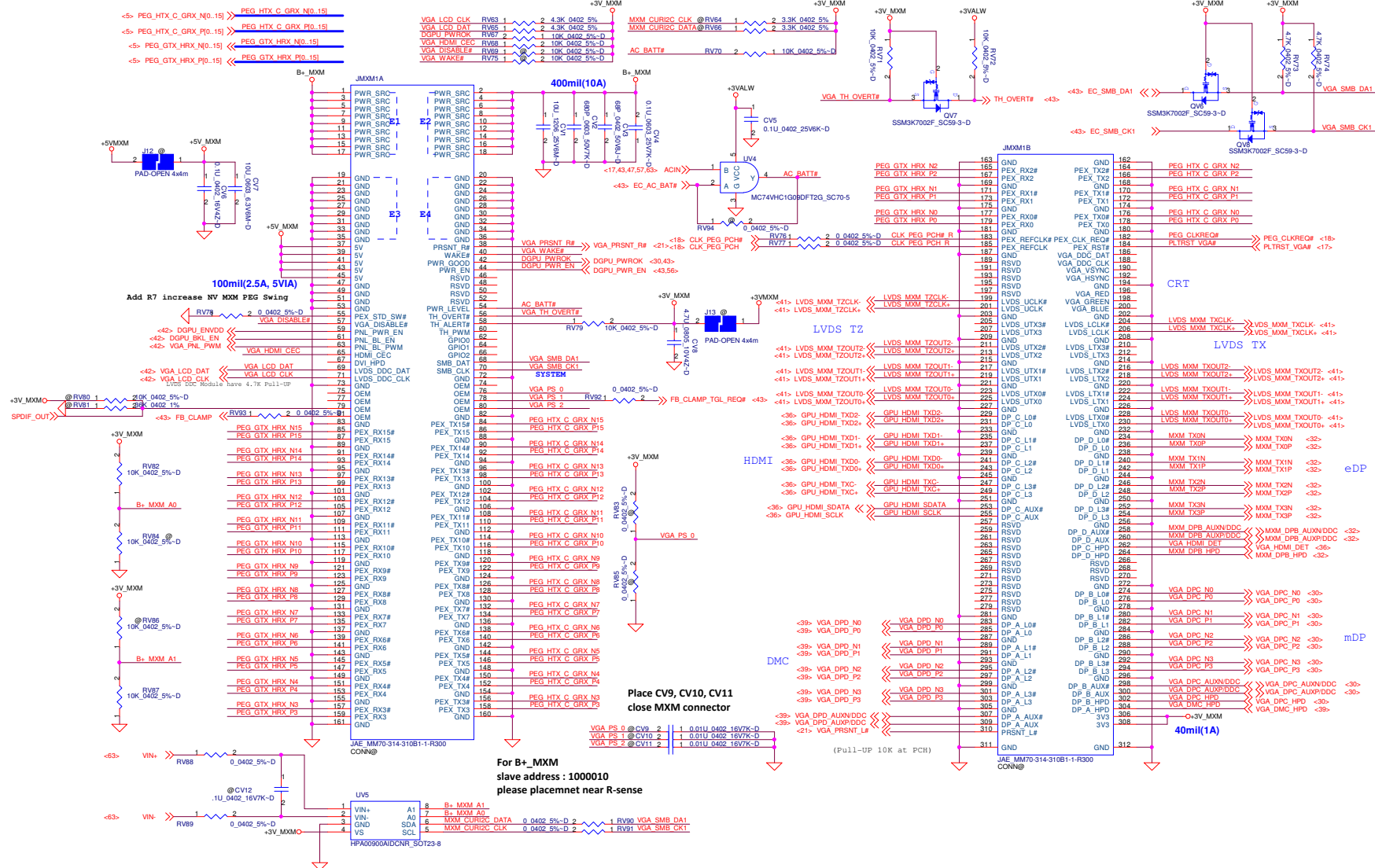




PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A







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				MXMIII Connector	
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				1	
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				Friday, June 22, 2012	
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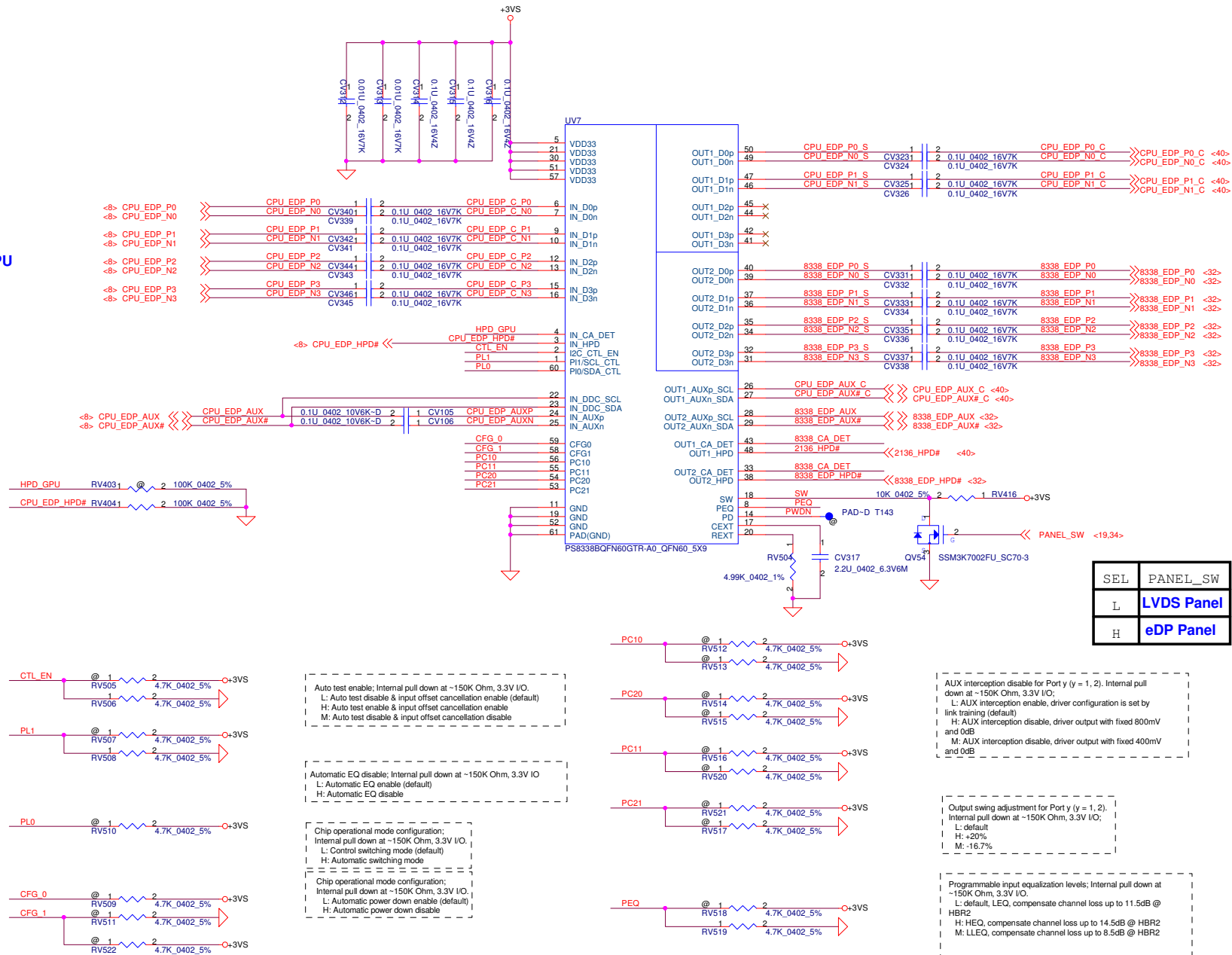
<b>Compal Electronics, Inc.</b>			
Title			
<b>Mini DP/Thunder Bolt power</b>			
EN R S	Doc u m e n t N u m b e r	Rev	0.1
DATE	LA-9331P		
Date	Friday, June 22, 2012	Sheet 27 of 61	

## CPU to EDP &amp; LVDS MUX

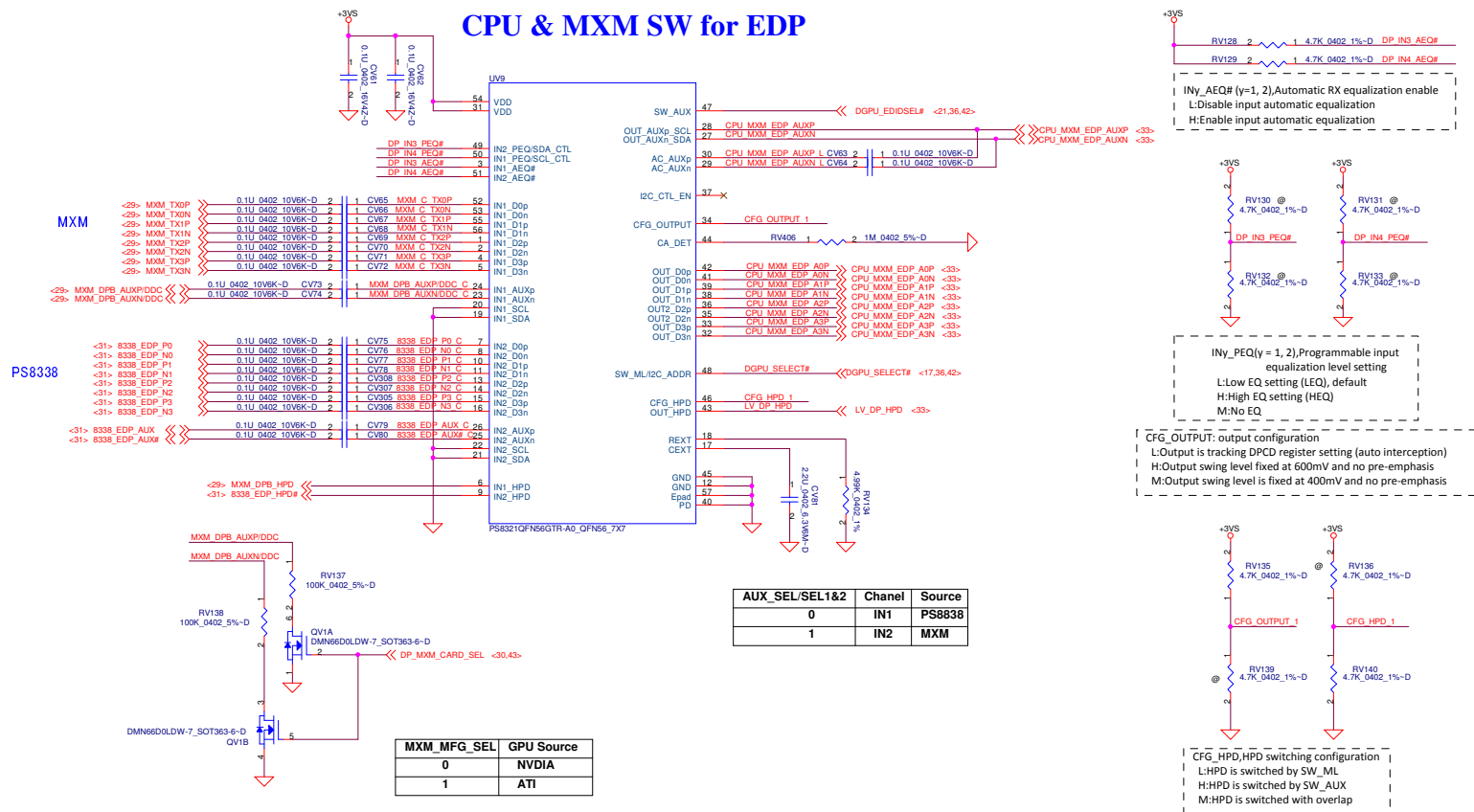
CPU

LVDS Panel

eDP Panel



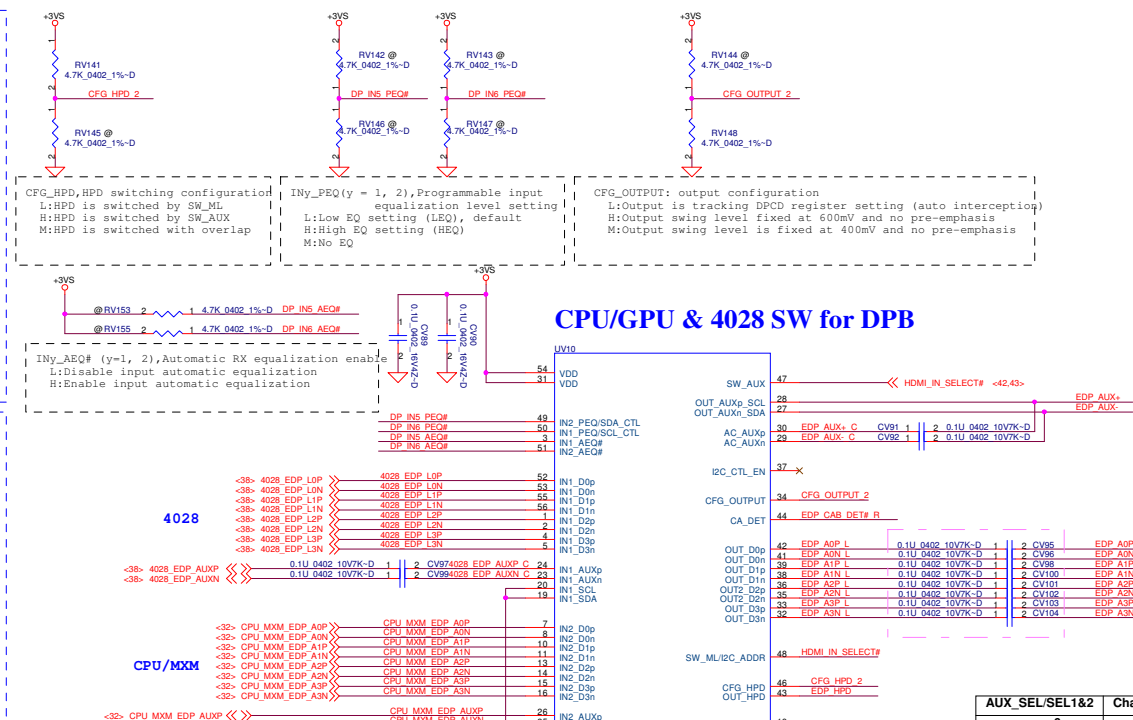
## CPU & MXM SW for EDP



AUX_SEL/SEL1&2	Chanel	Source
0	IN1	PS8838
1	IN2	MXM

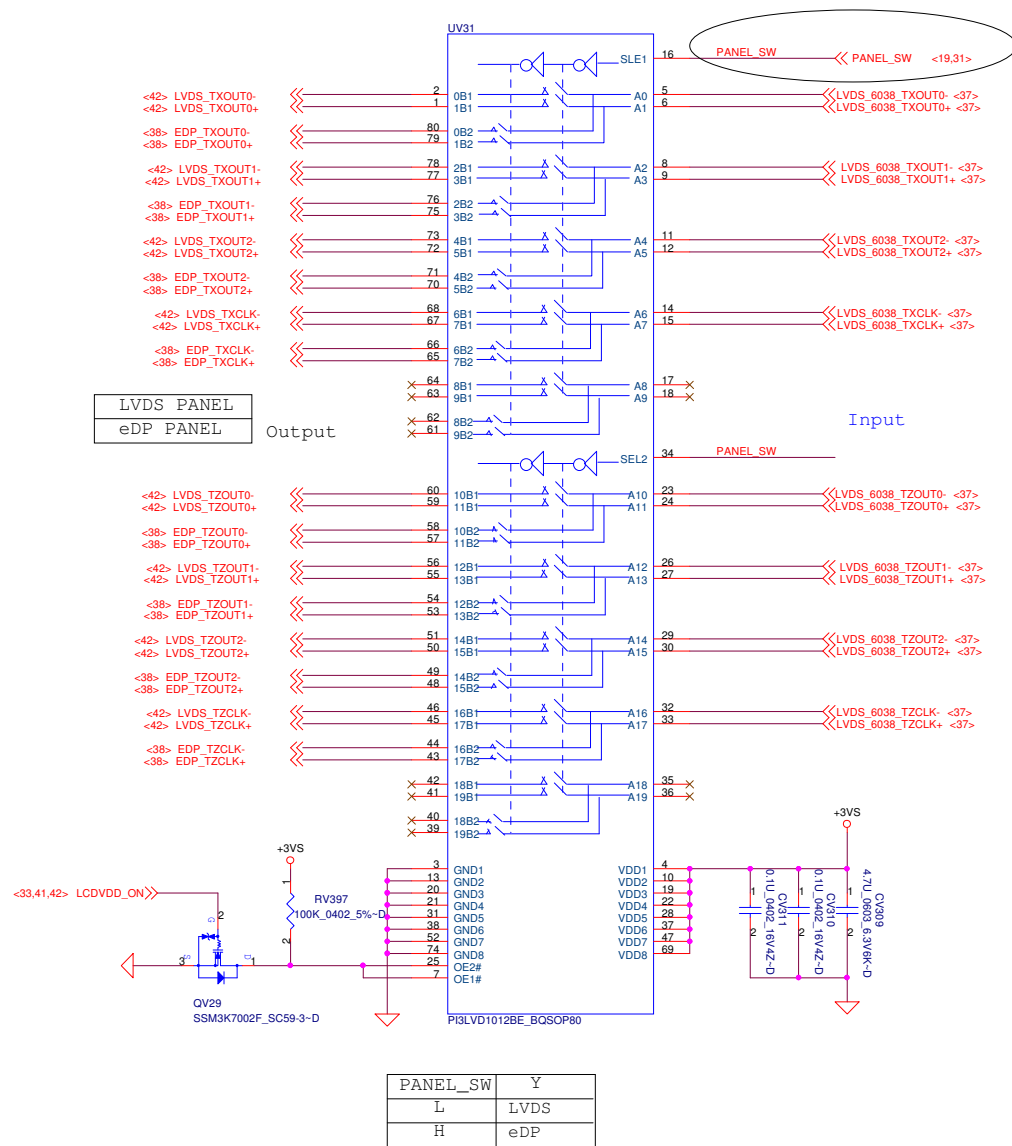
MXM_MFG_SEL	GPU Source
0	NVIDIA
1	ATI



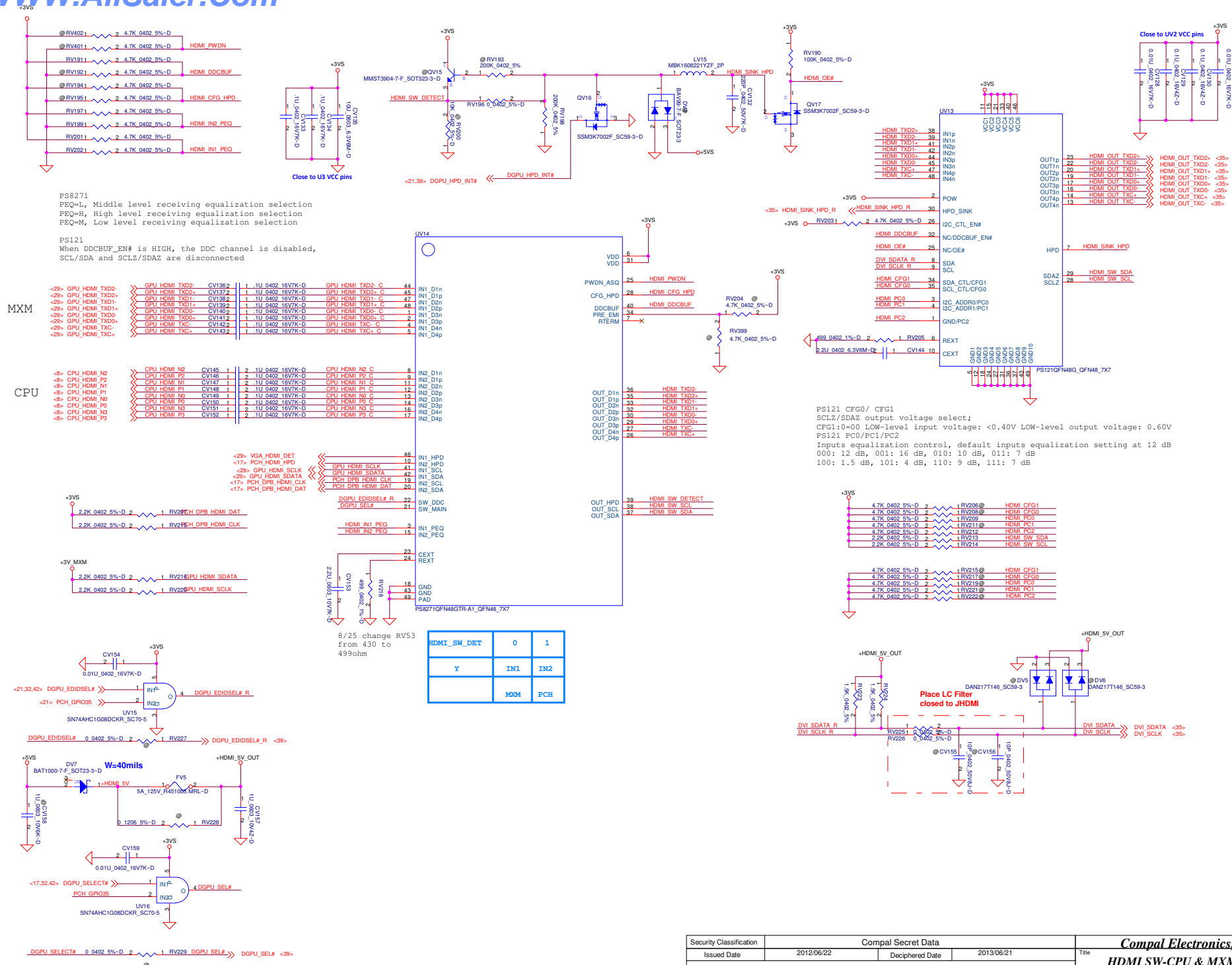
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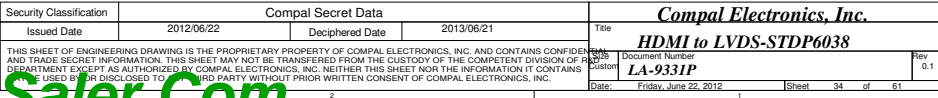
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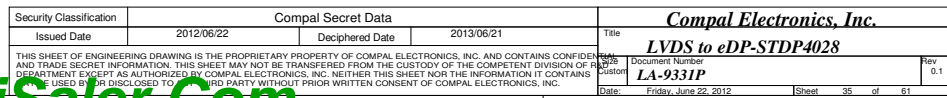
# STDP6038 to EDP & LVDS MUX



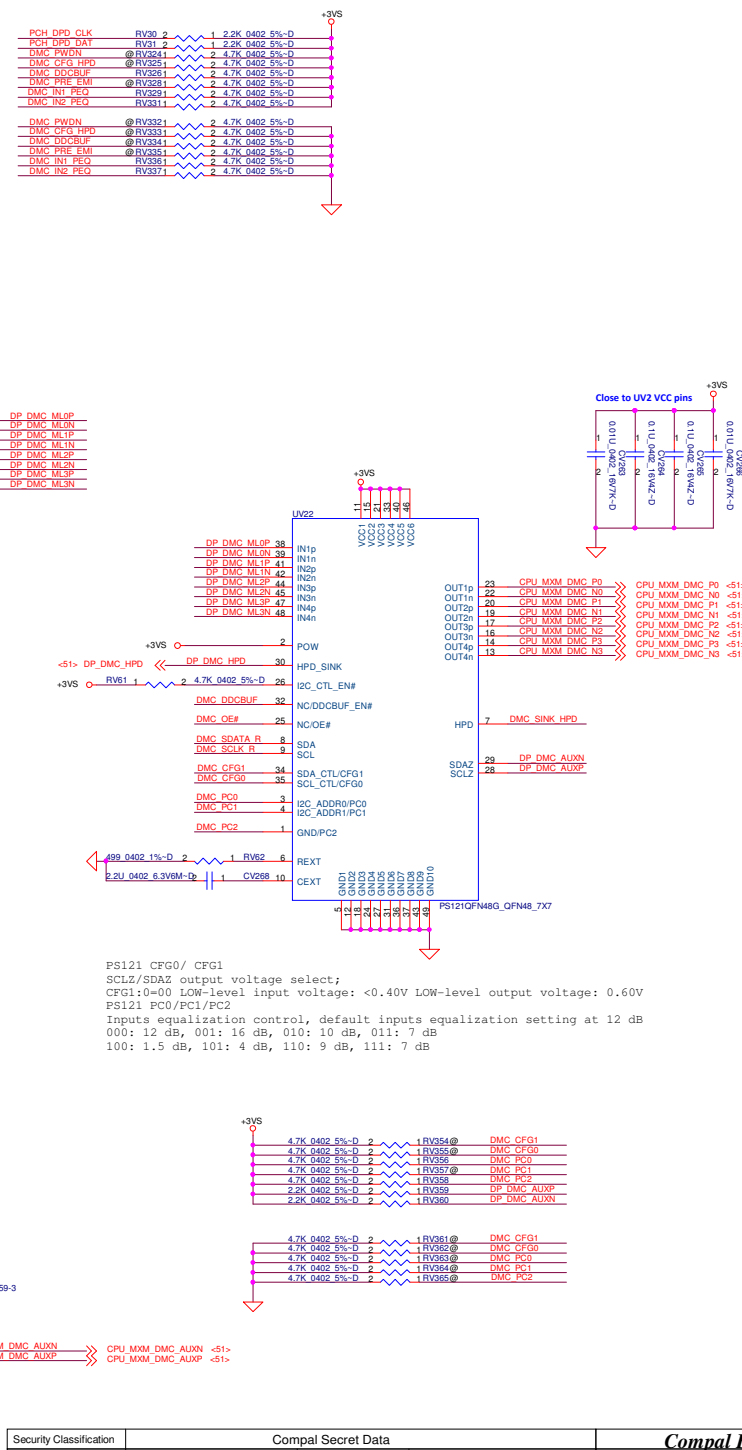






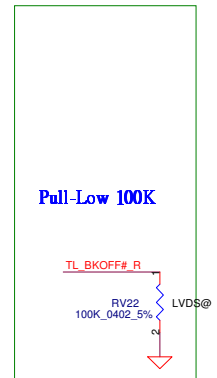
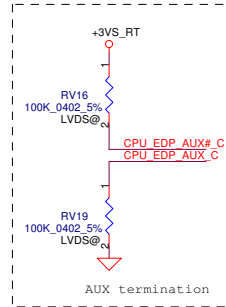
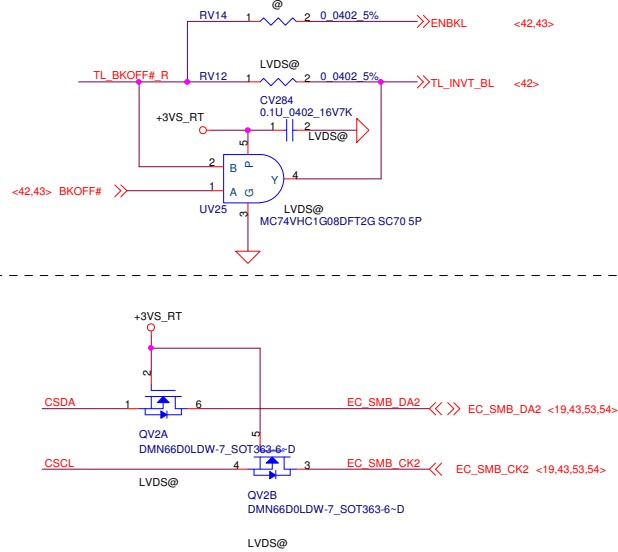
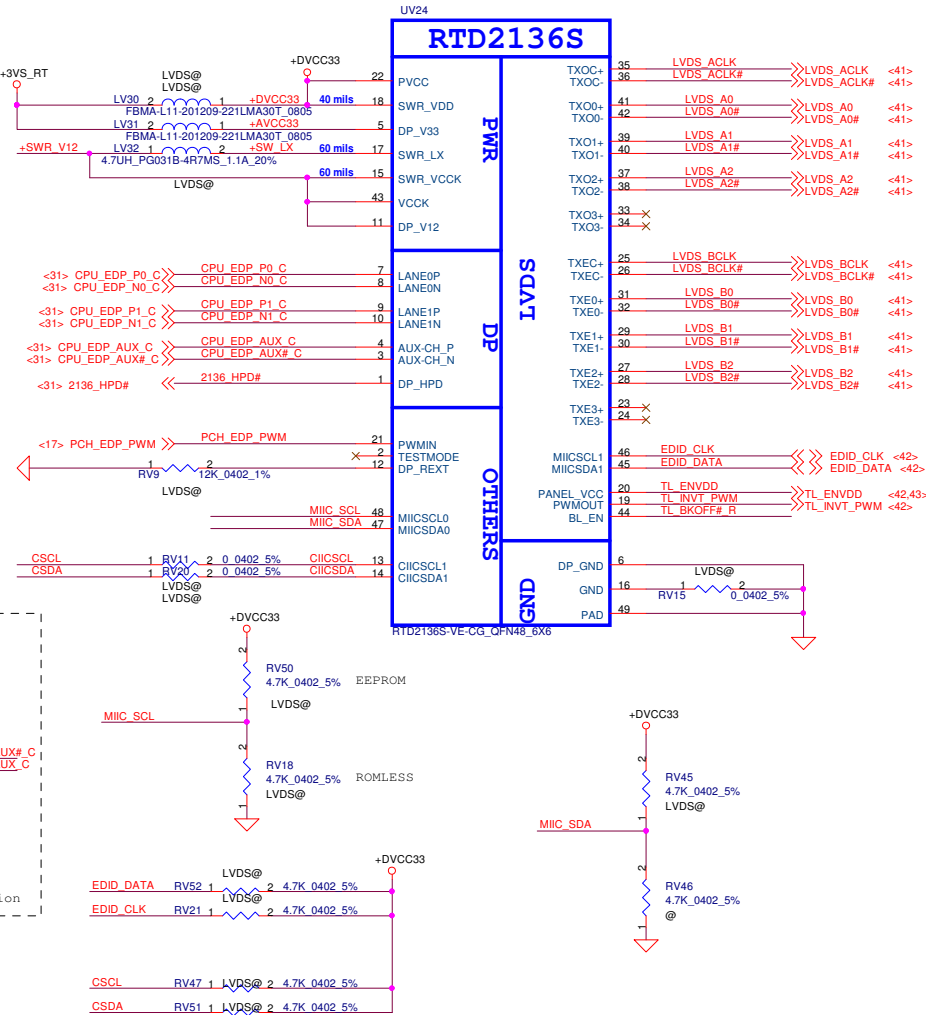
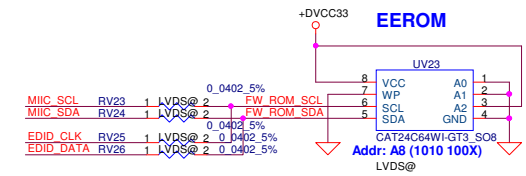






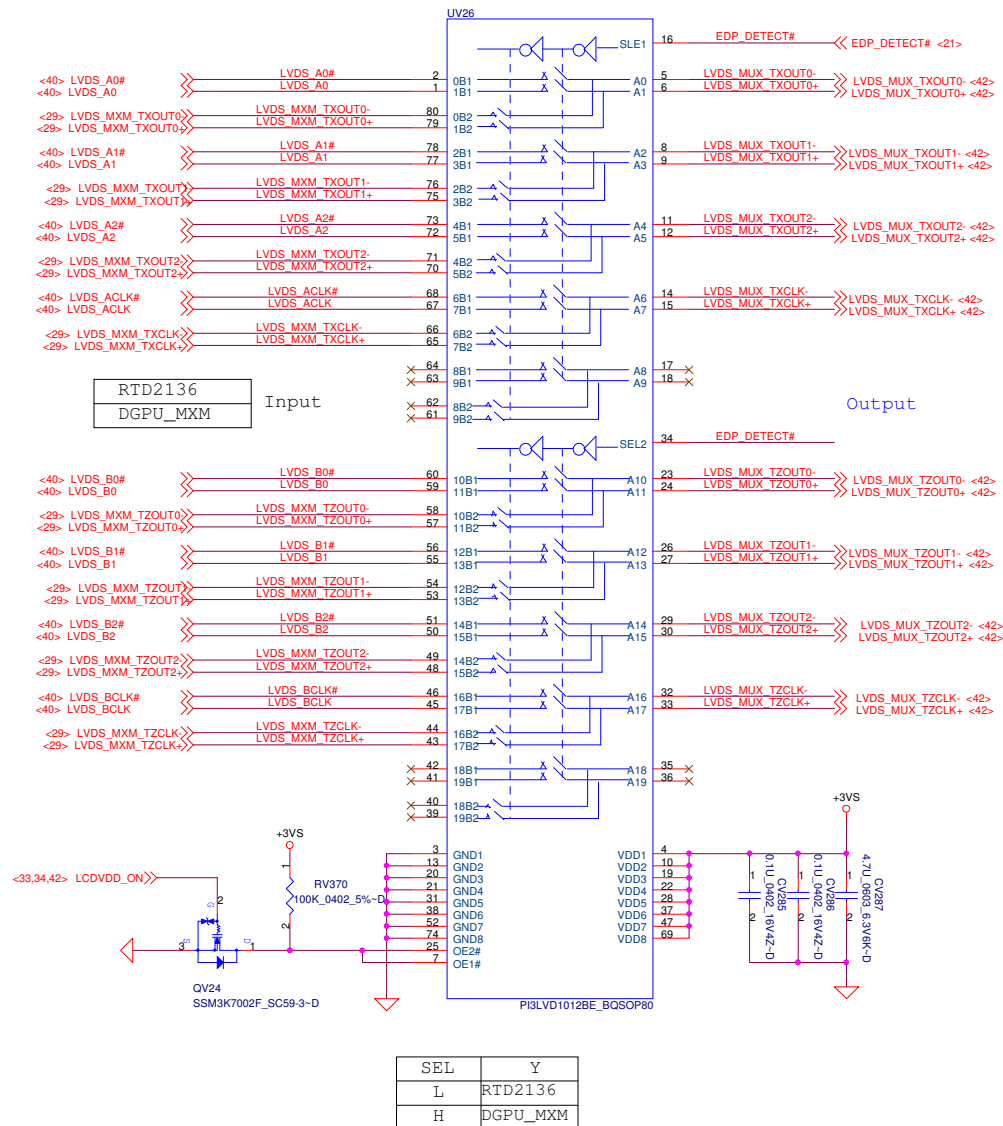
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Date: Friday, June 22, 2012				Sheet	37 of 61

## STDP6038 SW STDP4028 PCH/GPU AUX for LVDS

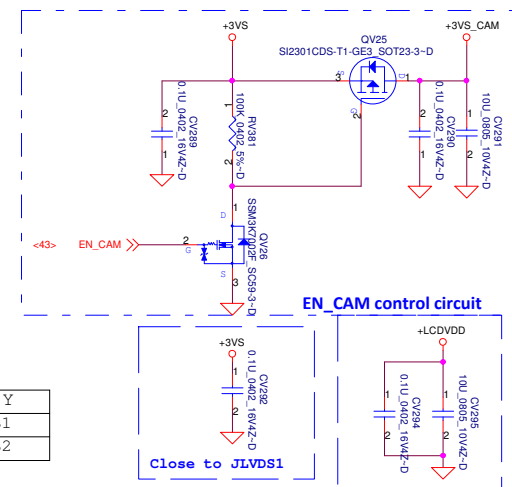


S1	S0	1A	2A	Y
0	0	1B1	2B1	HDMI IN (D)
0	1	1B2	2B2	DSC
1	0	1B3	2B3	HDMI IN (I)
1	1	1B4	2B4	UMA

CPU/MXM (MUX)
HDMI IN (1:2)

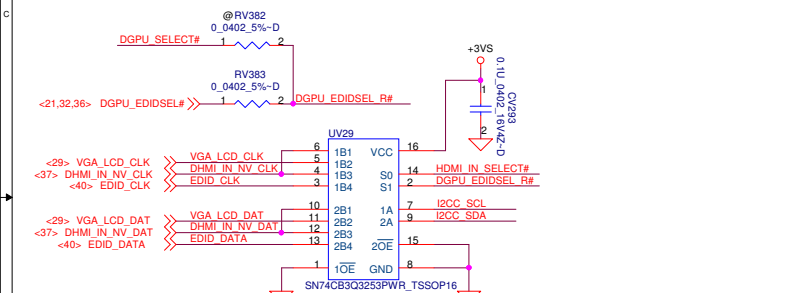
Input

## Output

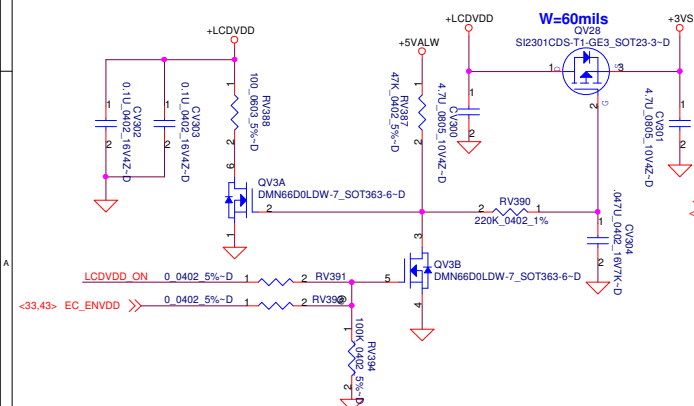
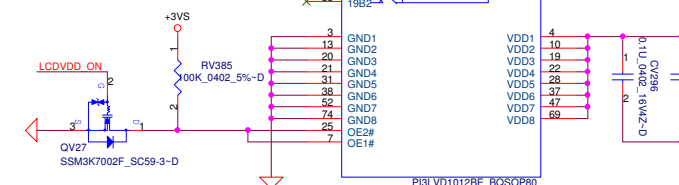


JLVDS1

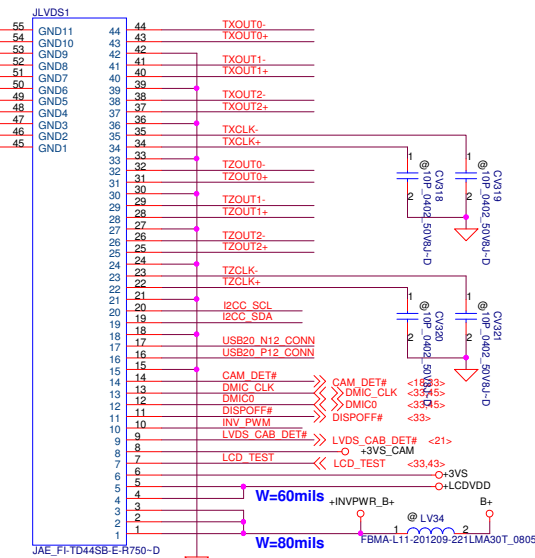
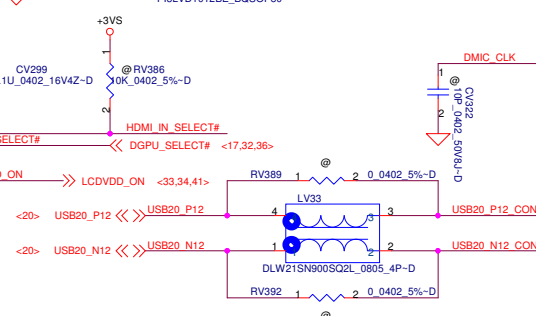
SEL	Y
L	B1
H	B2



S1	S0	1A	2A	Y
0	0	1B1	2B1	HDMI IN (D)
0	1	1B2	2B2	DSC
1	0	1B3	2B3	HDMI IN (I)
1	1	1B4	2B4	UMA



S1	S0	1A	2A	Y
0	0	1B1	2B1	HDMI IN
0	1	1B2	2B2	DSC
1	0	1B3	2B3	HDMI IN
1	1	1B4	2B4	UMA



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**Compal Electronics, Inc.**

LVDS SW- 6038/SYSTEM &amp; CONN

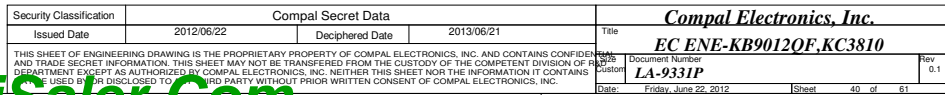
**LA-9331P**

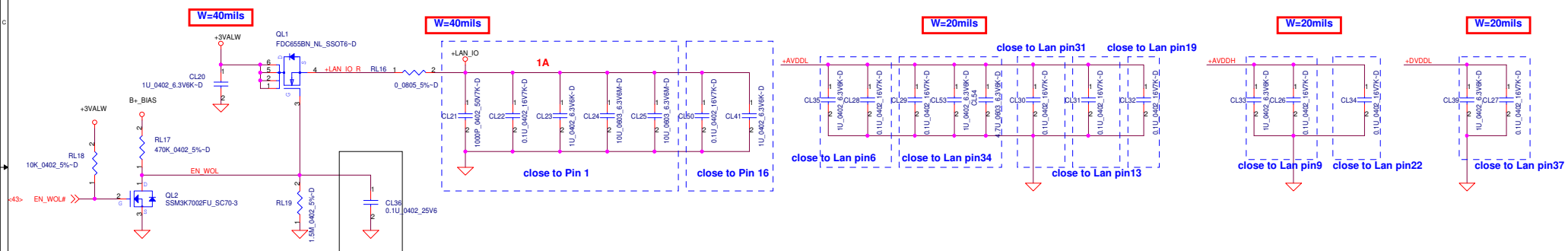
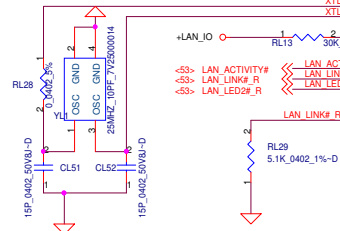
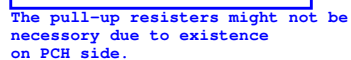
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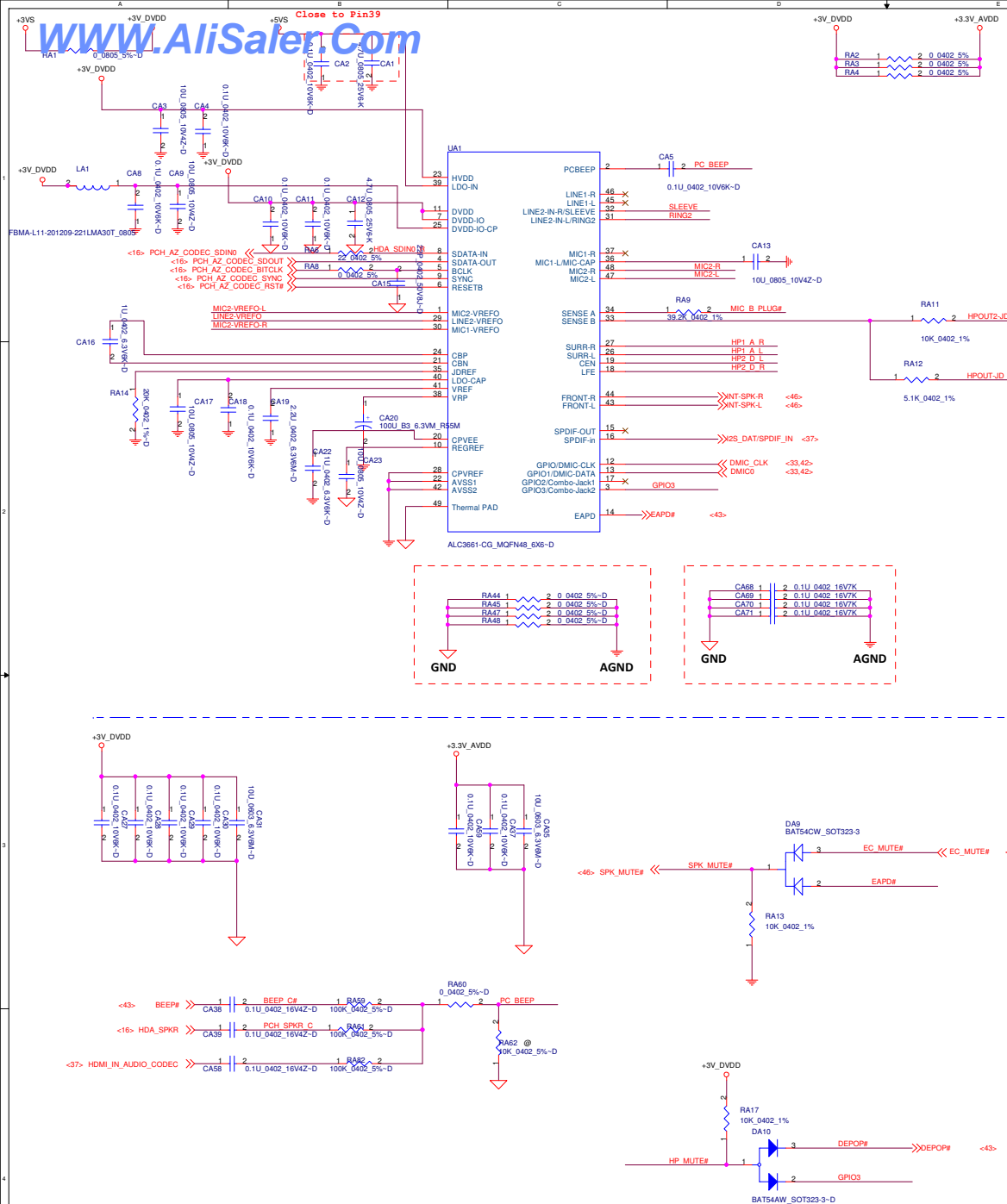
Date: Friday, June 22, 2012

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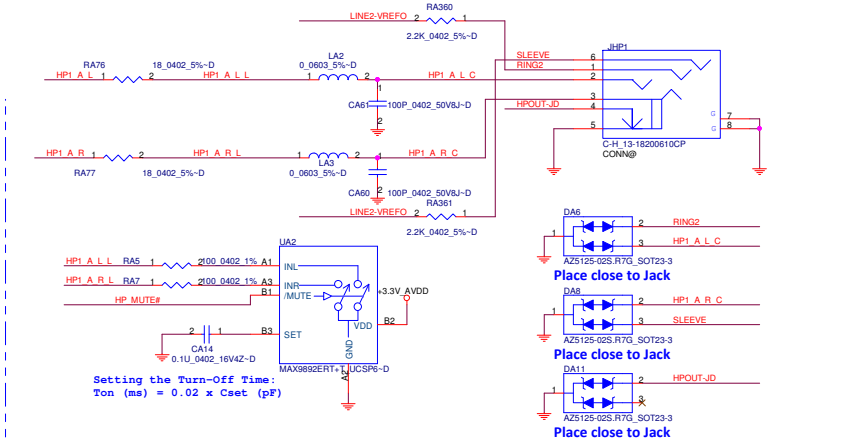
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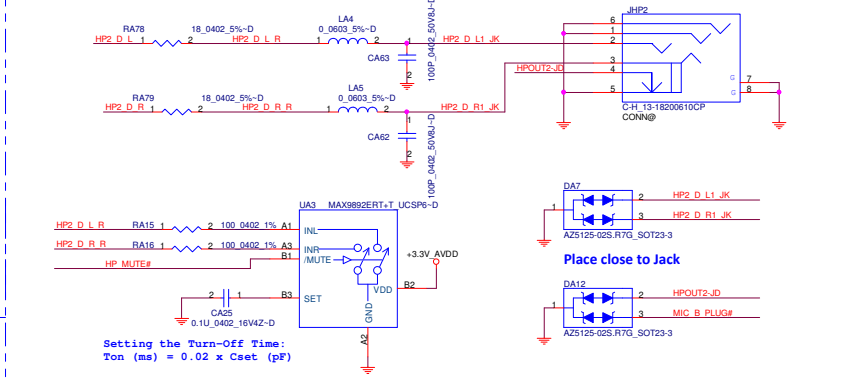




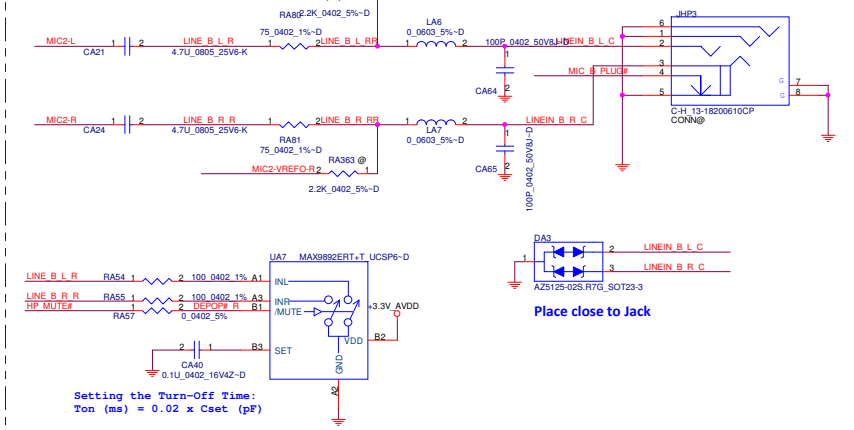
### S1 (Out + In) : Front L/R + HP1 + MIC (auto-sense)



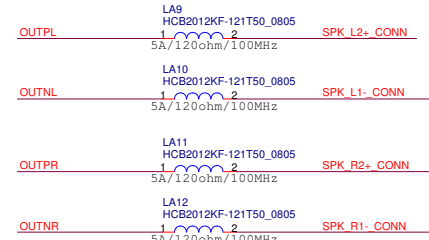
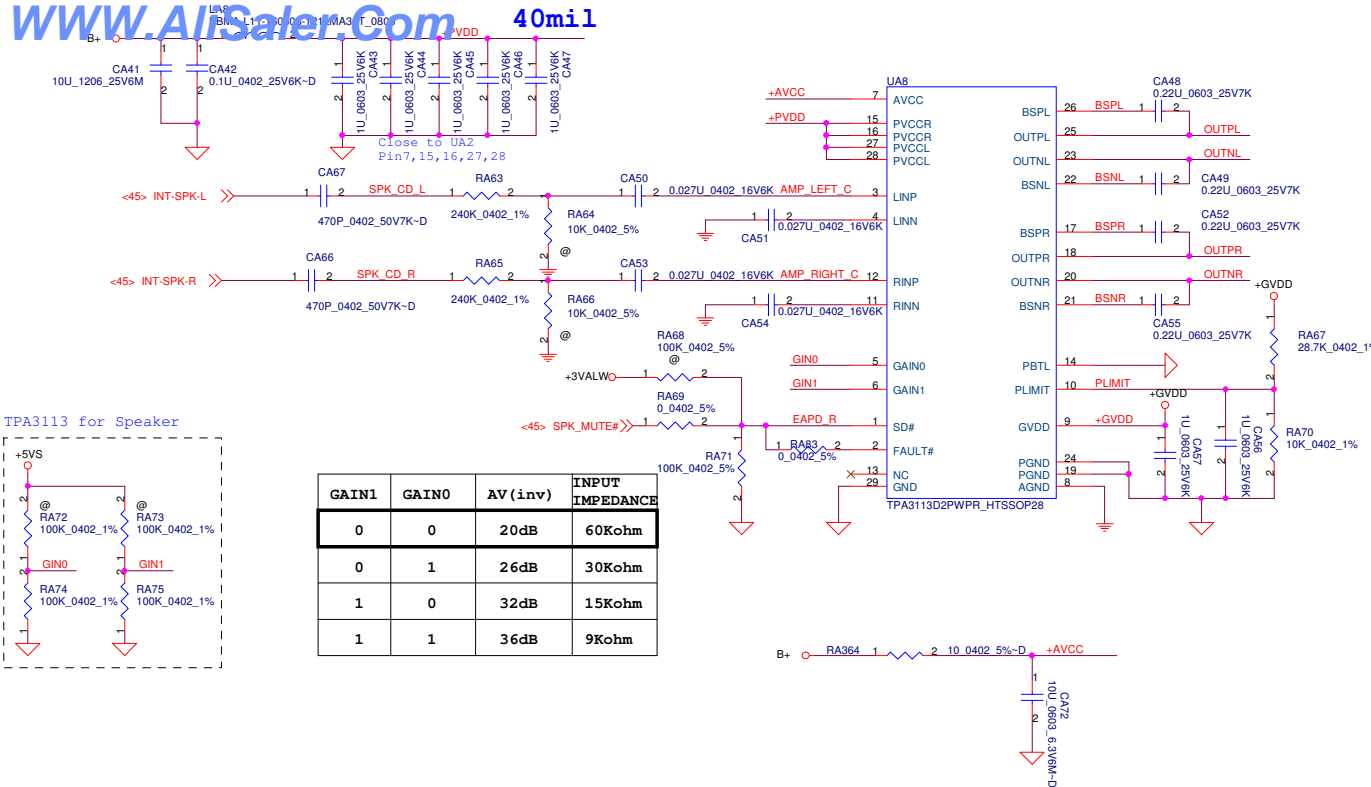
### S2 (Out) :Center + HP2



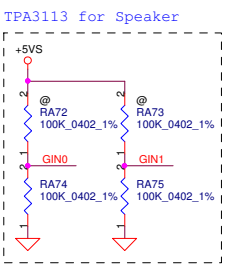
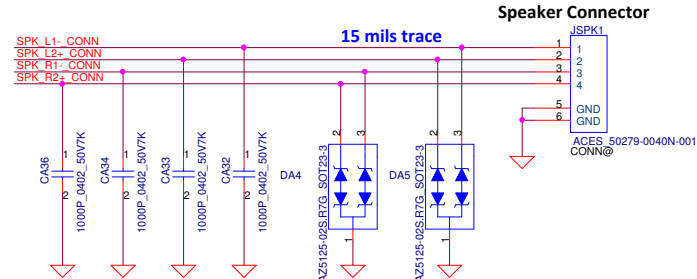
### S3 (Out) : Rear L/R



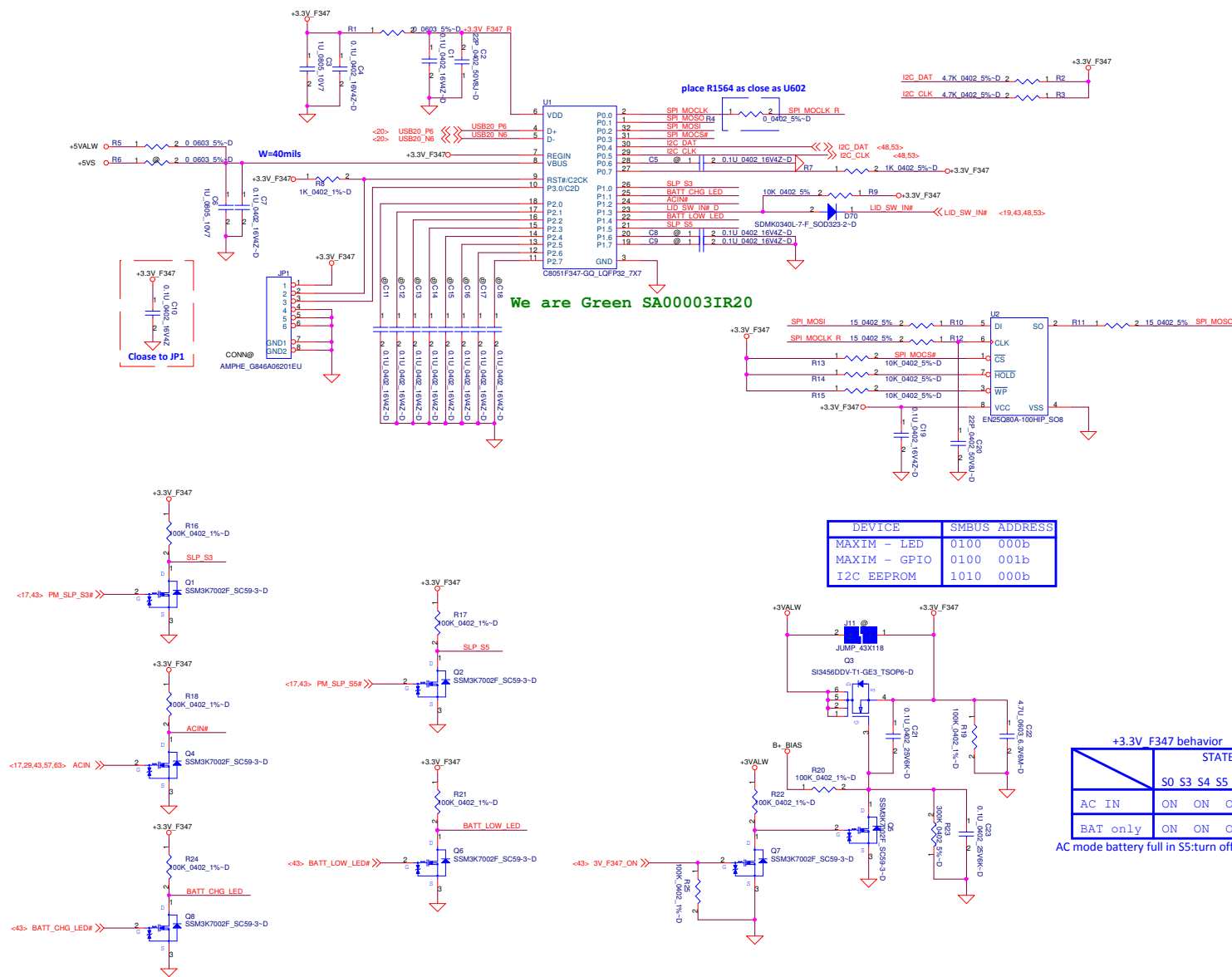
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Issued Date		Deciphered Date		2012/06/22	
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Document Number		LA-931P		Rev 0.1	
Date		Friday, June 22, 2012		Sheet 42 of 61	



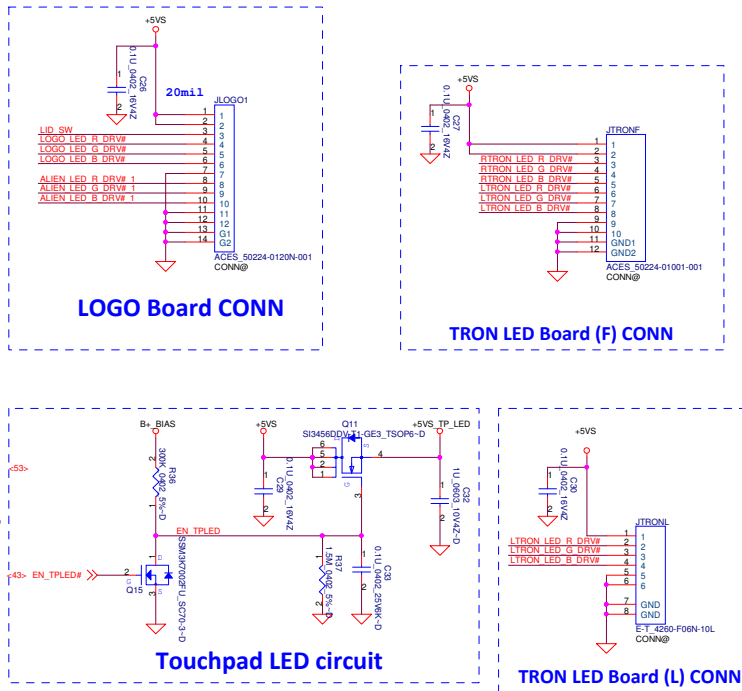
Speaker amp impedance of JBL is 4 ohm.



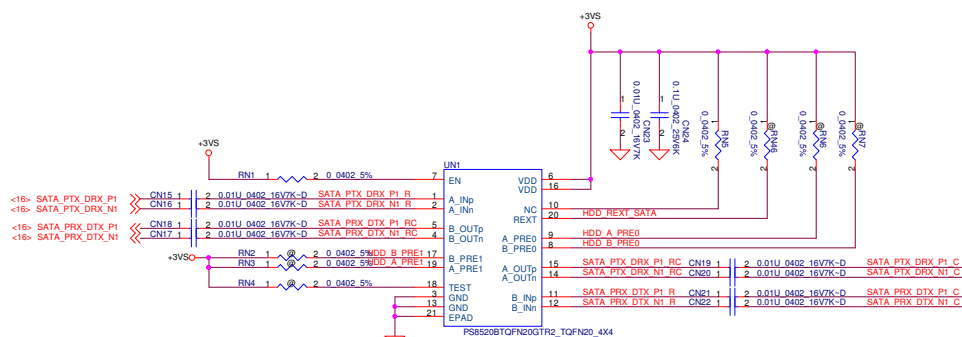
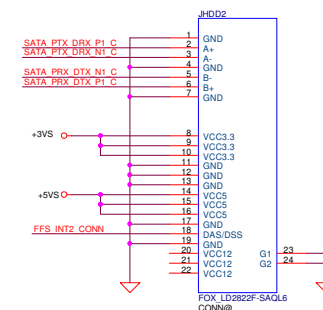
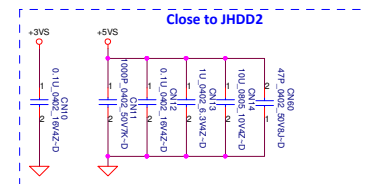
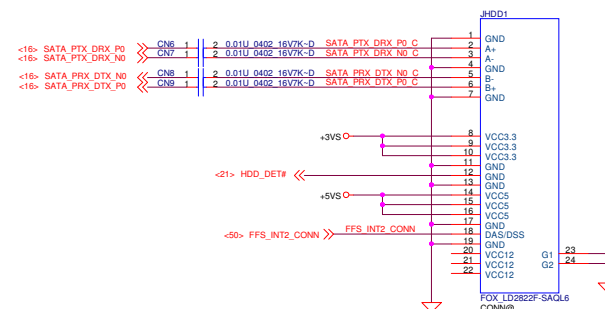
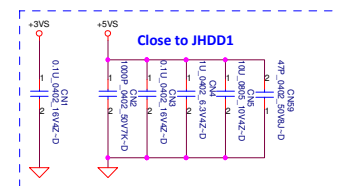
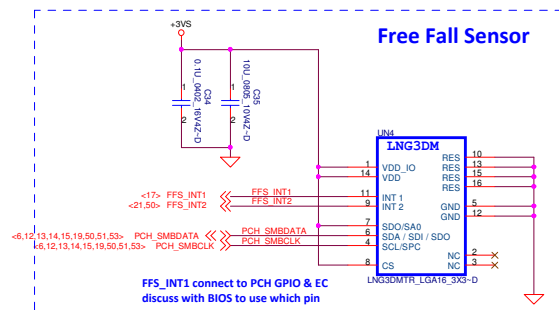








Reference	AD2	AD1	AD0	MAX7313
U605	0	1	0	Tron Lights, TP A-panel, B-Panel Logo
U608	0	1	1	Power Button, Media and Status LED Color
U?	1	0	0	Button, Indicator Brightness



Pin 20:  
PARADE PS8250B:  
Reserve RN46, Mount RN12

PERICOM PI3EQX6741ST:  
Mount RN46, Reserve RN12

ASMEDIA ASM1466:  
Mount RN46, Reserve RN12

Pin 9:  
PARADE PS8250B:  
Reserve RN11.

PERICOM PI3EQX6741ST:  
Reserve RN11

ASMEDIA ASM1466:  
Mount RN11 to pull down

HDD\_B\_PRE0 RN8 1 2 0.0402 5%

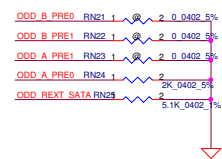
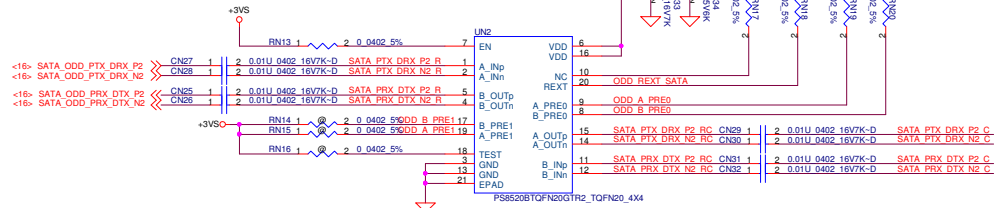
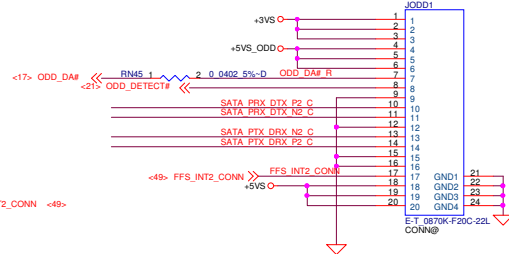
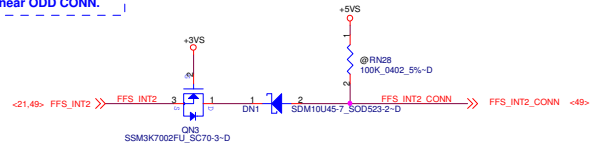
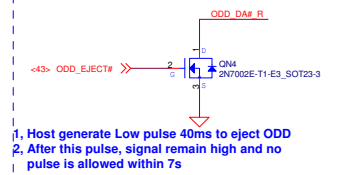
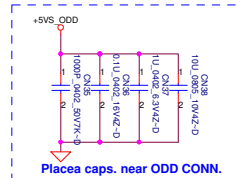
HDD\_B\_PRE1 RN9 1 2 0.0402 5%

HDD\_A\_PRE1 RN10 1 2 0.0402 5%

HDD\_A\_PRE0 RN11 1 2 0.0402 5%

HDD\_REXT SATA RN12 1 2 5.1K 0402 5%

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Pin 20:  
PARADE PS8250B:  
Reserve RN18, Mount RN25

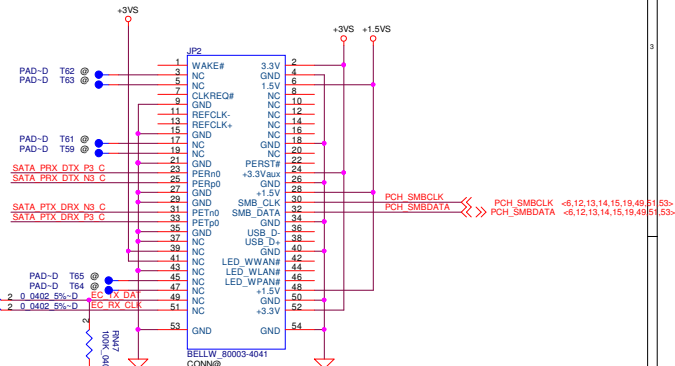
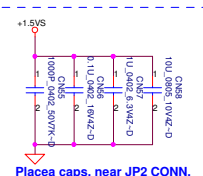
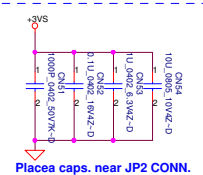
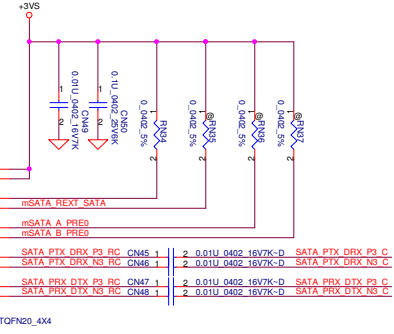
PERICOM PI3EQX6741ST:  
Mount RN18, Reserve RN25

ASMEDIA ASM1466:  
Mount RN18, Reserve RN25

Pin 9:  
PARADE PS8250B:  
Reserve RN24.

PERICOM PI3EQX6741ST:  
Reserve RN24

ASMEDIA ASM1466:  
Mount RN24 to pull down



Pin 20:  
PARADE PS8250B:  
Reserve RN35, Mount RN42

PERICOM PI3EQX6741ST:  
Mount RN35, Reserve RN42

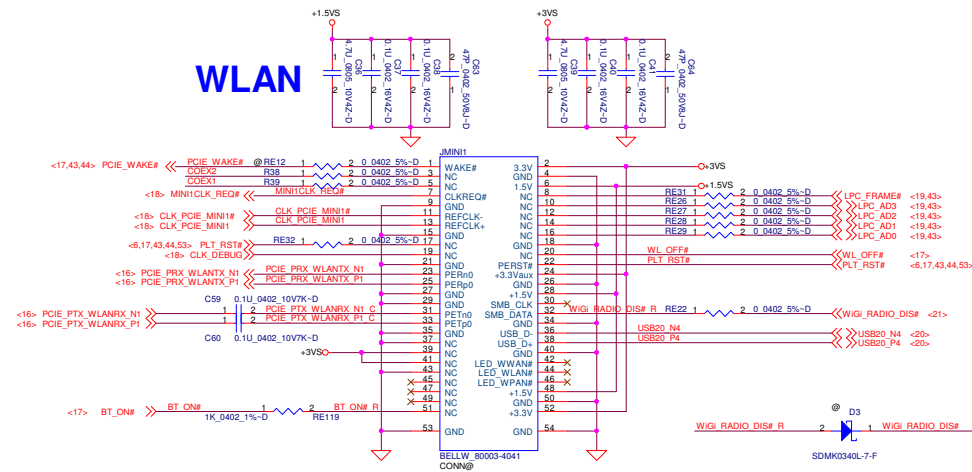
ASMEDIA ASM1466:  
Mount RN35, Reserve RN42

Pin 9:  
PARADE PS8250B:  
Reserve RN41.

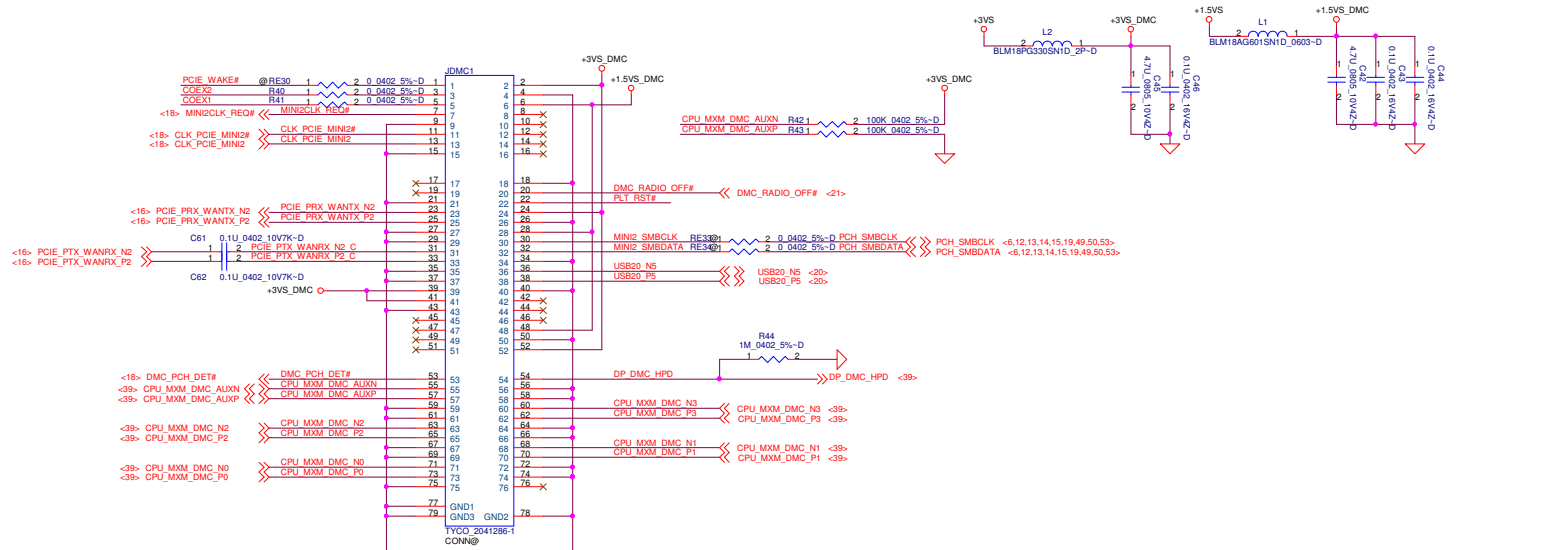
PERICOM PI3EQX6741ST:  
Reserve RN41

ASMEDIA ASM1466:  
Mount RN41 to pull down

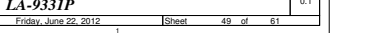
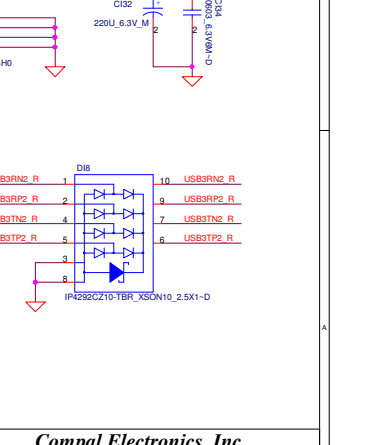
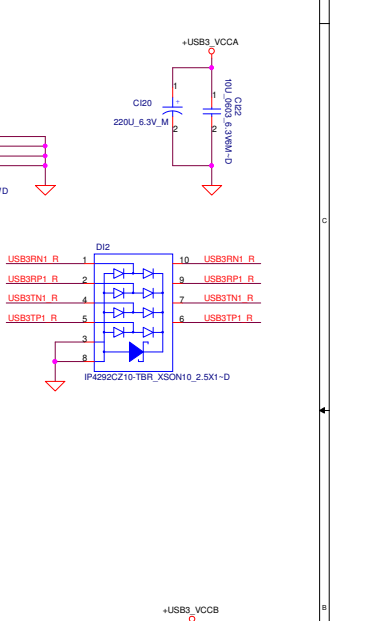
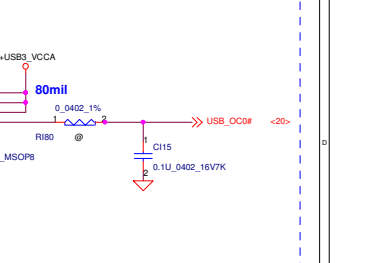
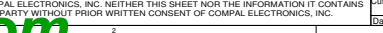
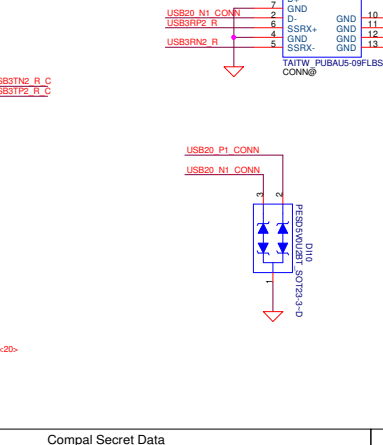
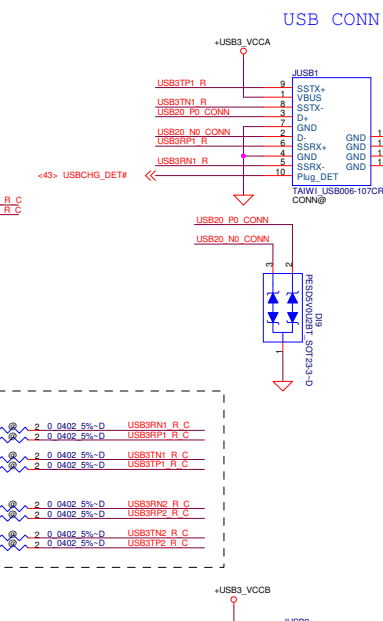
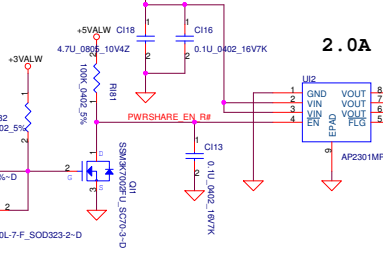
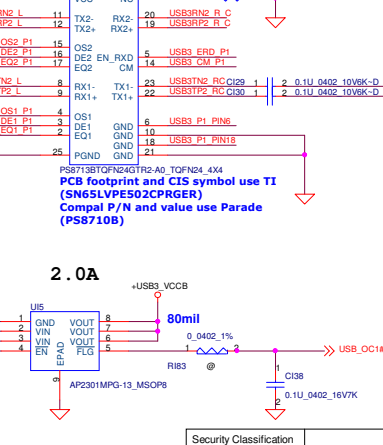
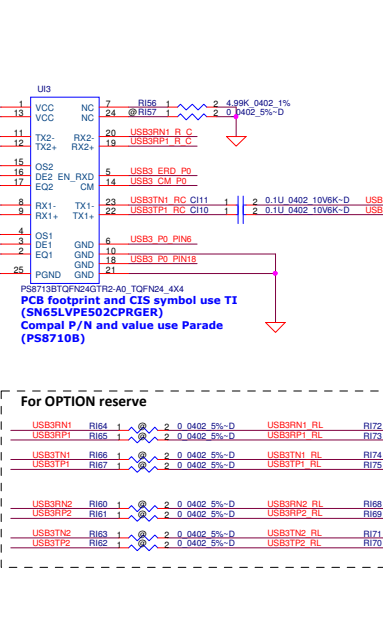
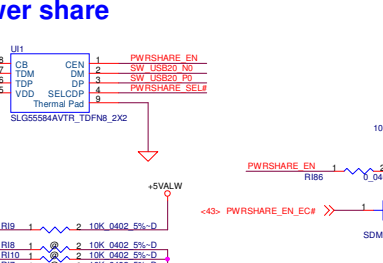
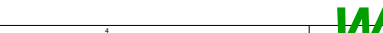
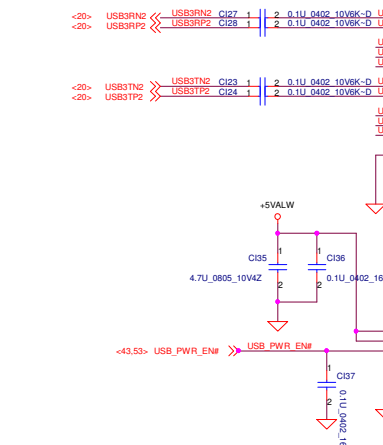
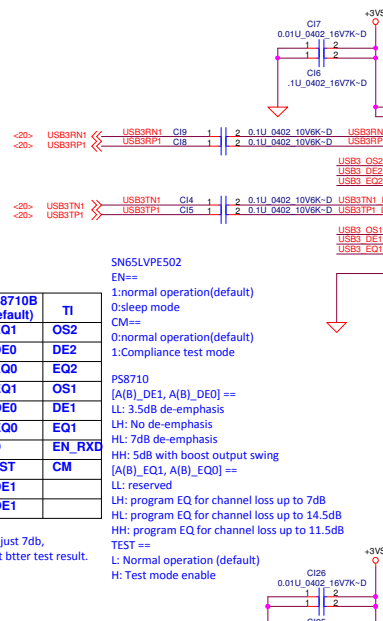
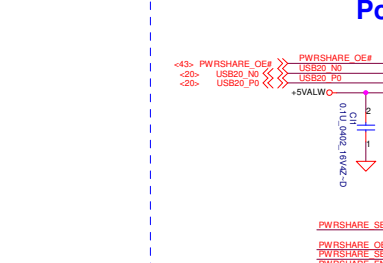
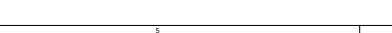
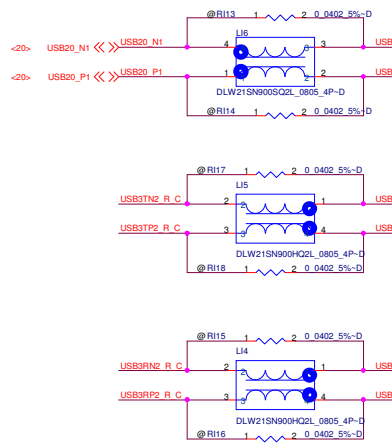
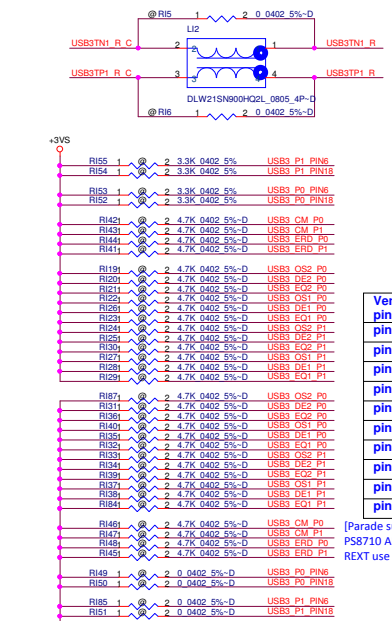
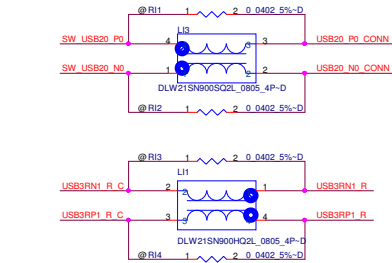
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## Display Mini Card (DMC)



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## Power share

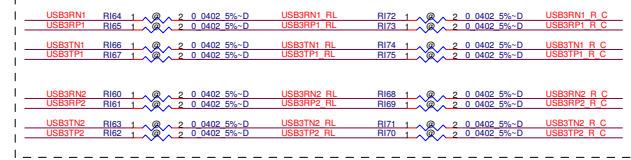
2.0A

## USB CONN

Vendor pin	PS8710B (default)	TI
pin15	AEQ1	OS2
pin16	ADE0	DE2
pin17	AEQ0	EQ2
pin4	BEQ1	OS1
pin3	BDE0	DE1
pin2	BEQ0	EQ1
pin5	PD	EN_RXD
pin14	TEST	CM
pin18	ADE1	
pin6	BDE1	

[Parade suggest]  
PS8710 AEQ0,BEQ0 adjust 7db,  
REXT use 3.3 K well get better test result.

## For OPTION reserve



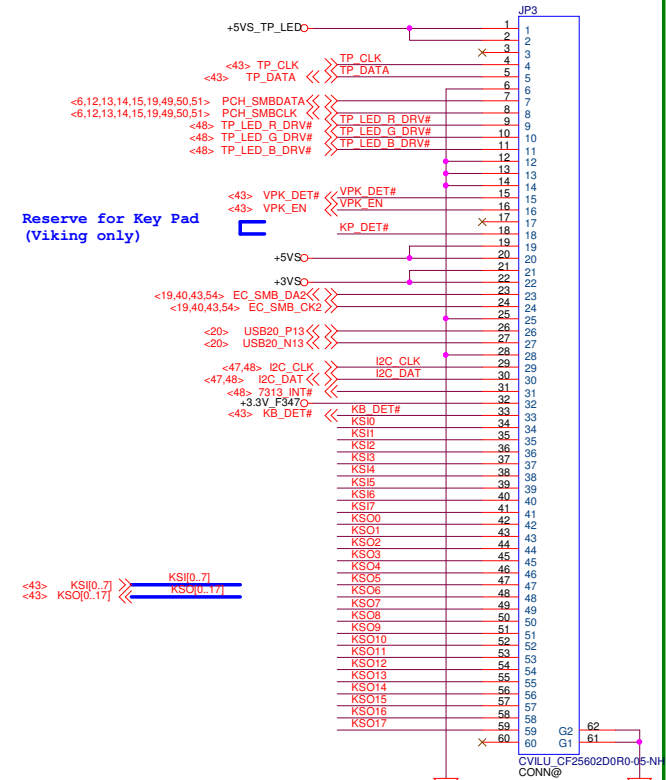
## For OPTION reserve



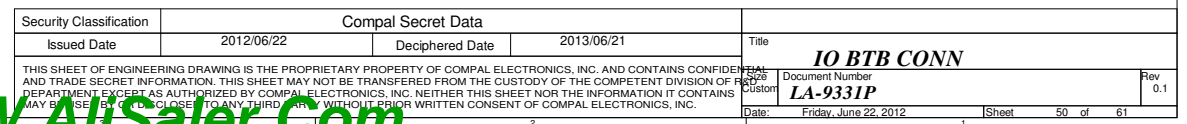
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Issued Date	2012/06/22	Deciphered Date	2013/06/21	

Compal Electronics, Inc.	
USB 3.0/2.0 x2 (left side)	
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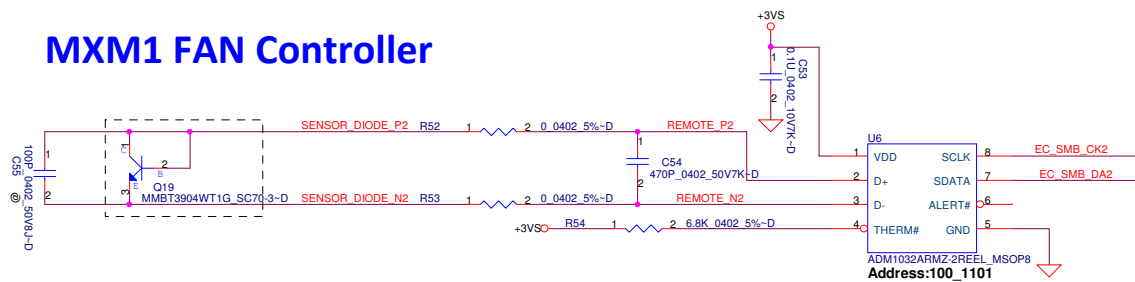
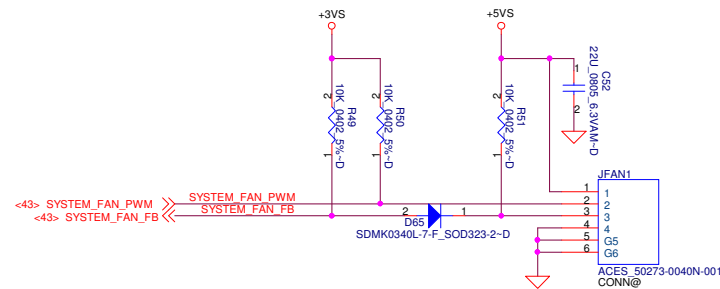
60 pin FFC connector To MB



### 30pin Connector to CardReader

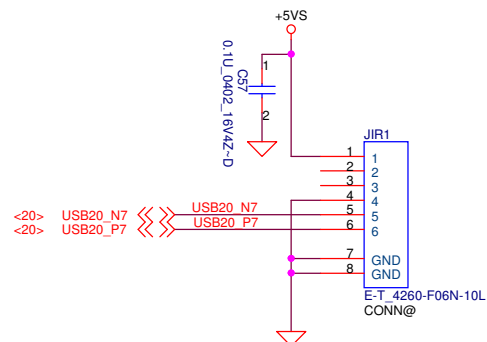


## MXM1 FAN Controller

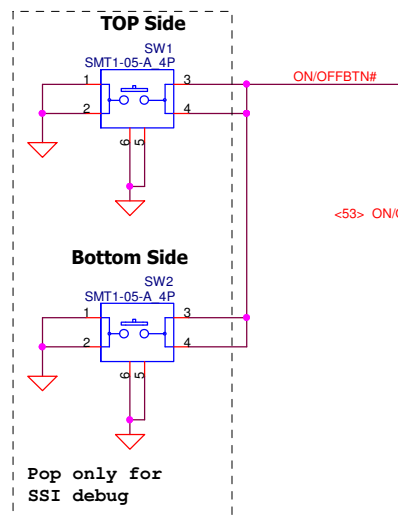


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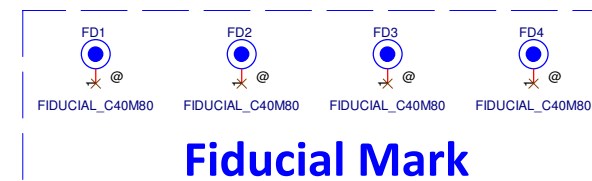
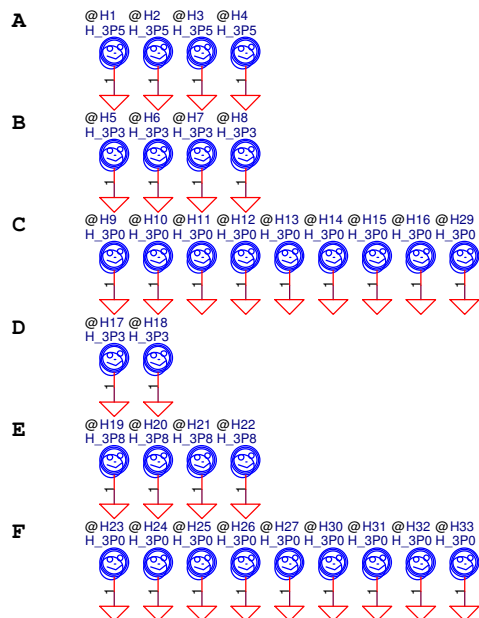
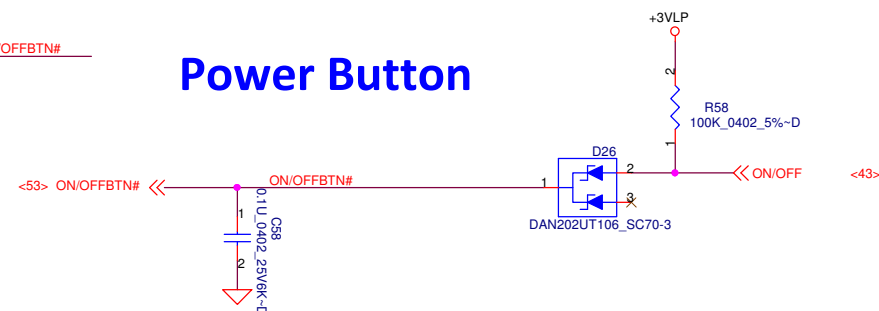
## IR SENSOR connector



## ON/OFF switch



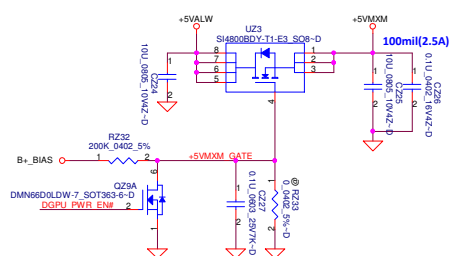
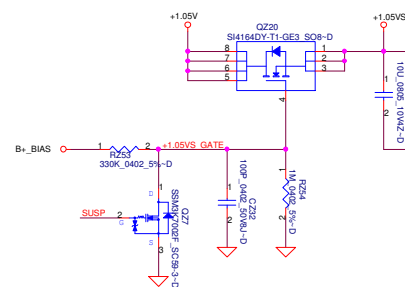
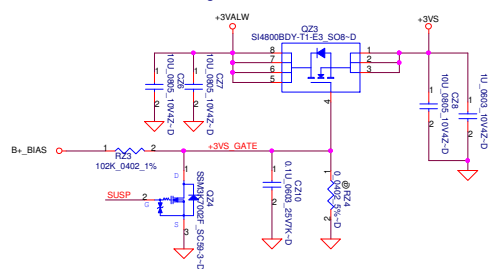
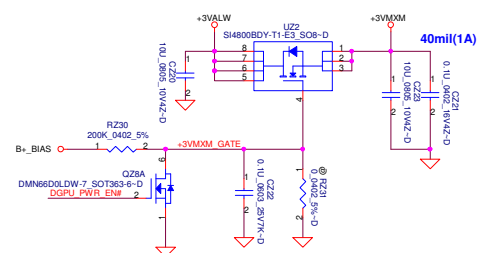
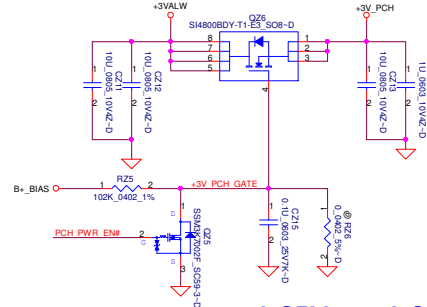
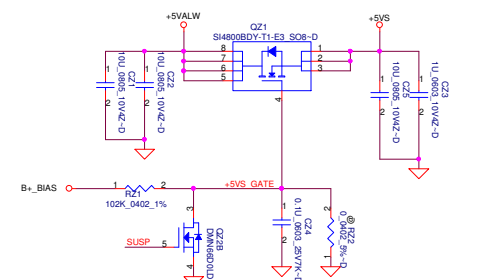
## Power Button



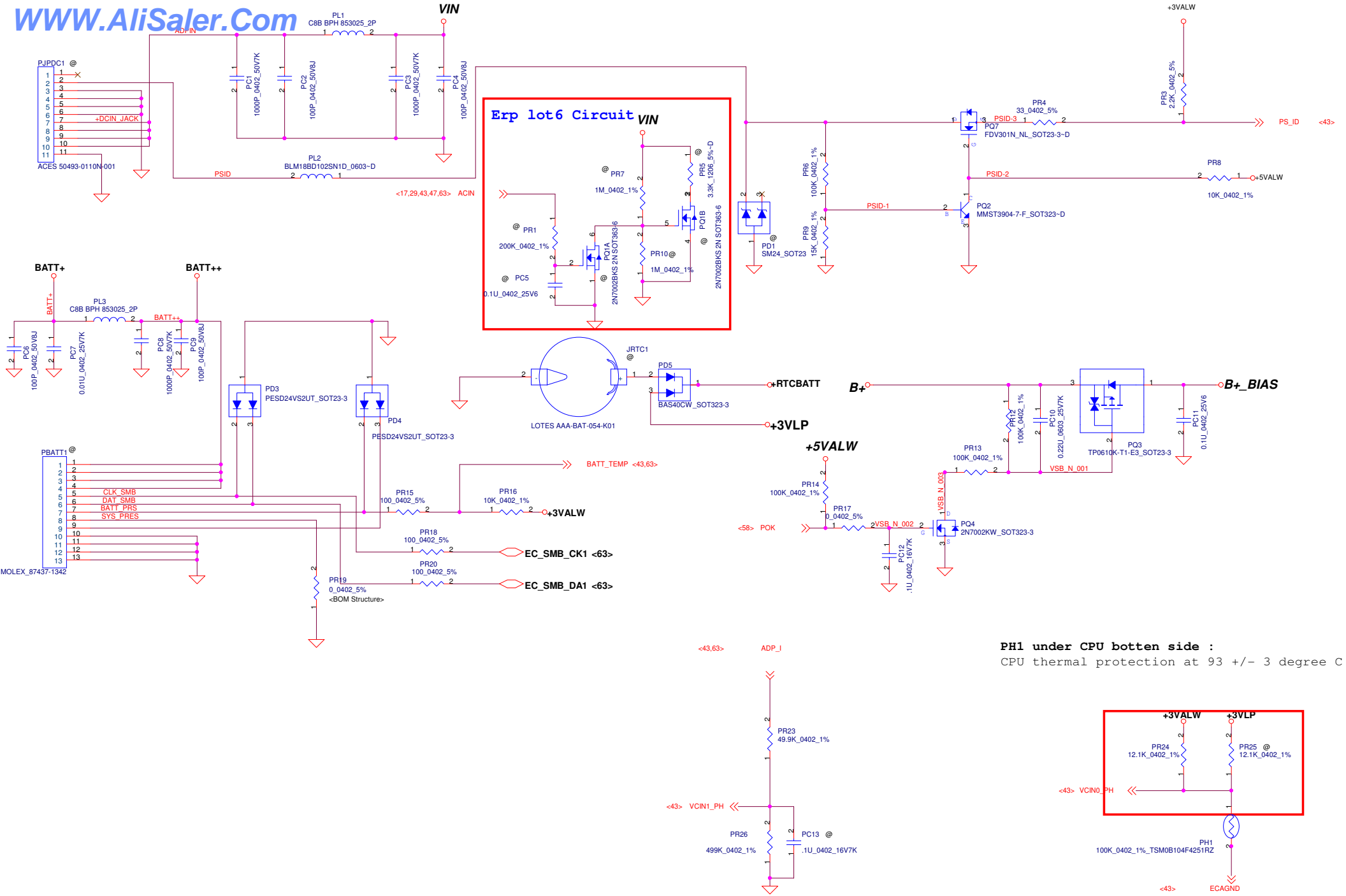
## Fiducial Mark

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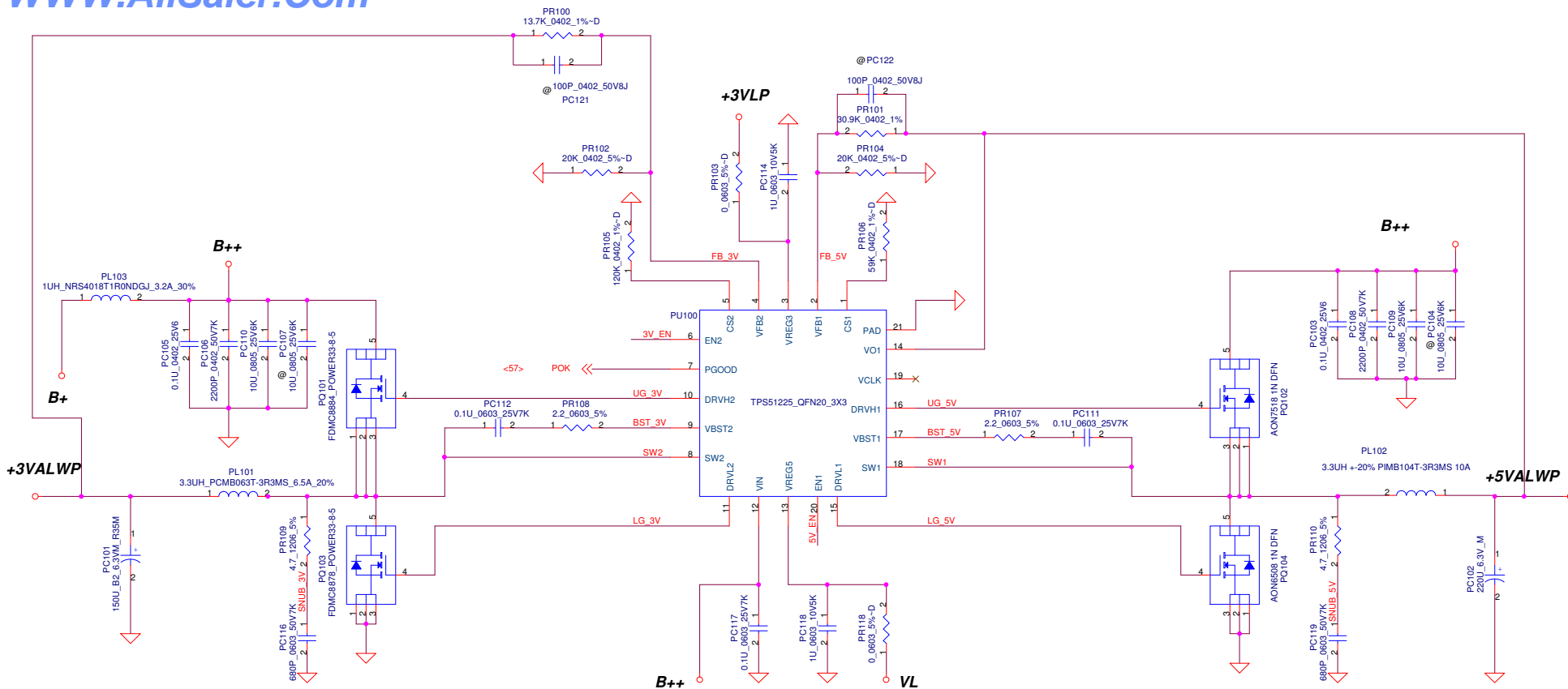




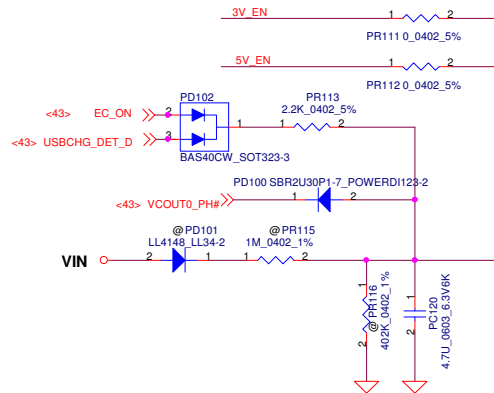
WWW.AliSaler.Com



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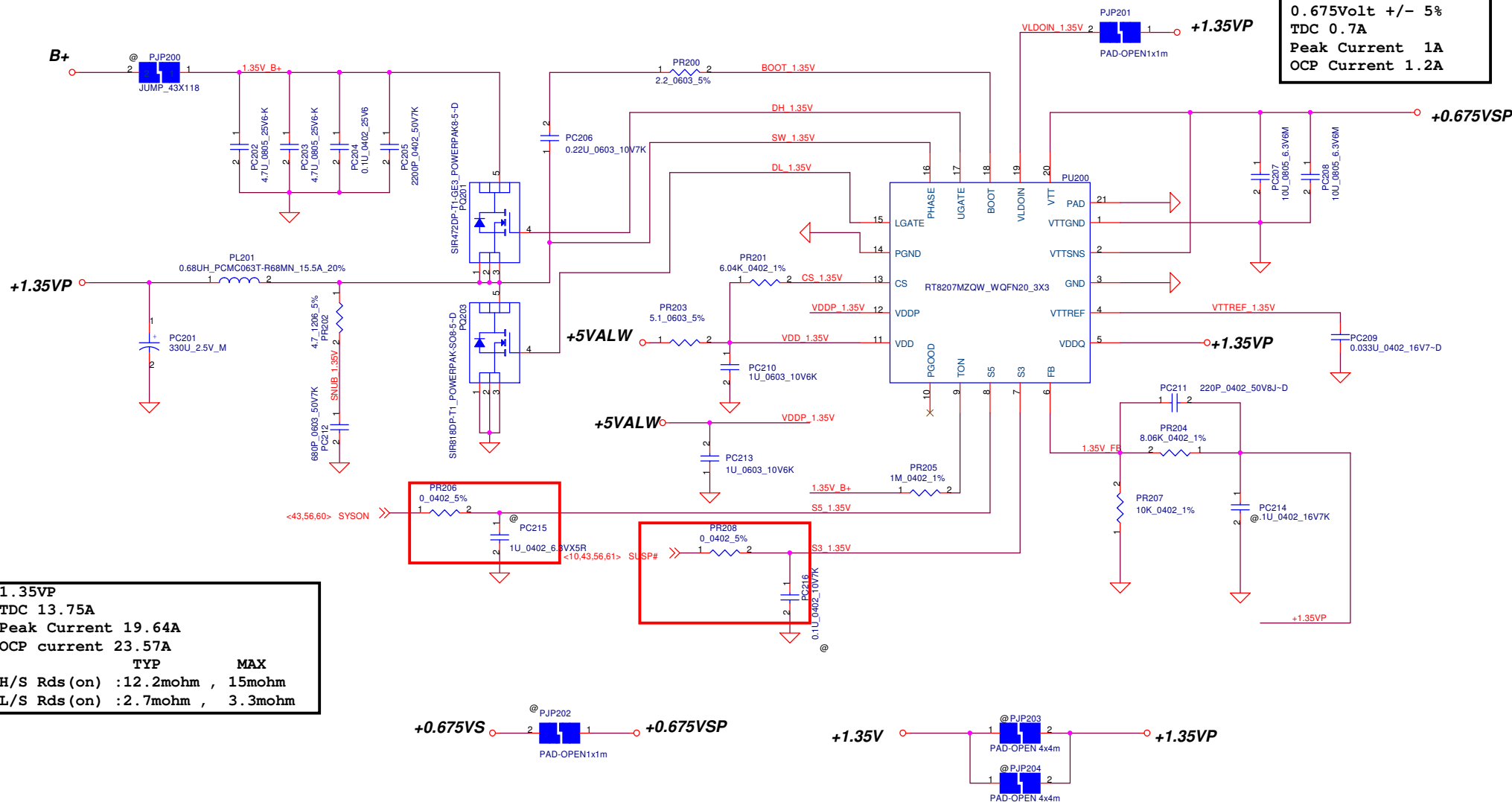


**3VALWP**  
TDC 6.08A  
Peak Current 8.11A  
OCP current 9.73A  
TYP MAX  
H/S Rds(on) :22mohm , 30mohm  
L/S Rds(on) :12.1mohm ,17mohm

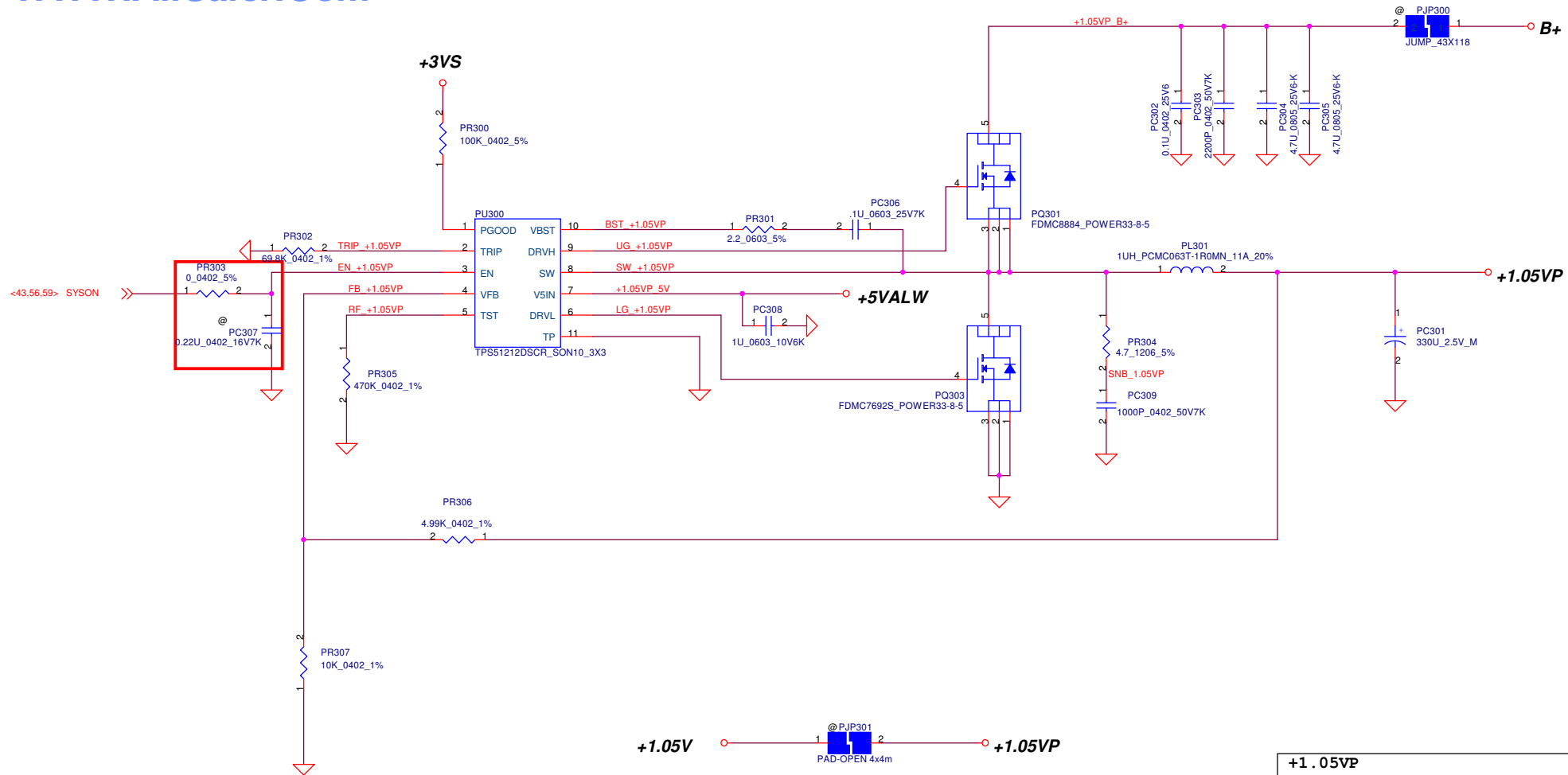


**5VALWP**  
TDC 10.64A  
Peak Current 14.19A  
OCP current 17.03A  
TYP MAX  
H/S Rds(on) 11.2mohm , 14mohm  
L/S Rds(on) :3.7mohm , 5mohm

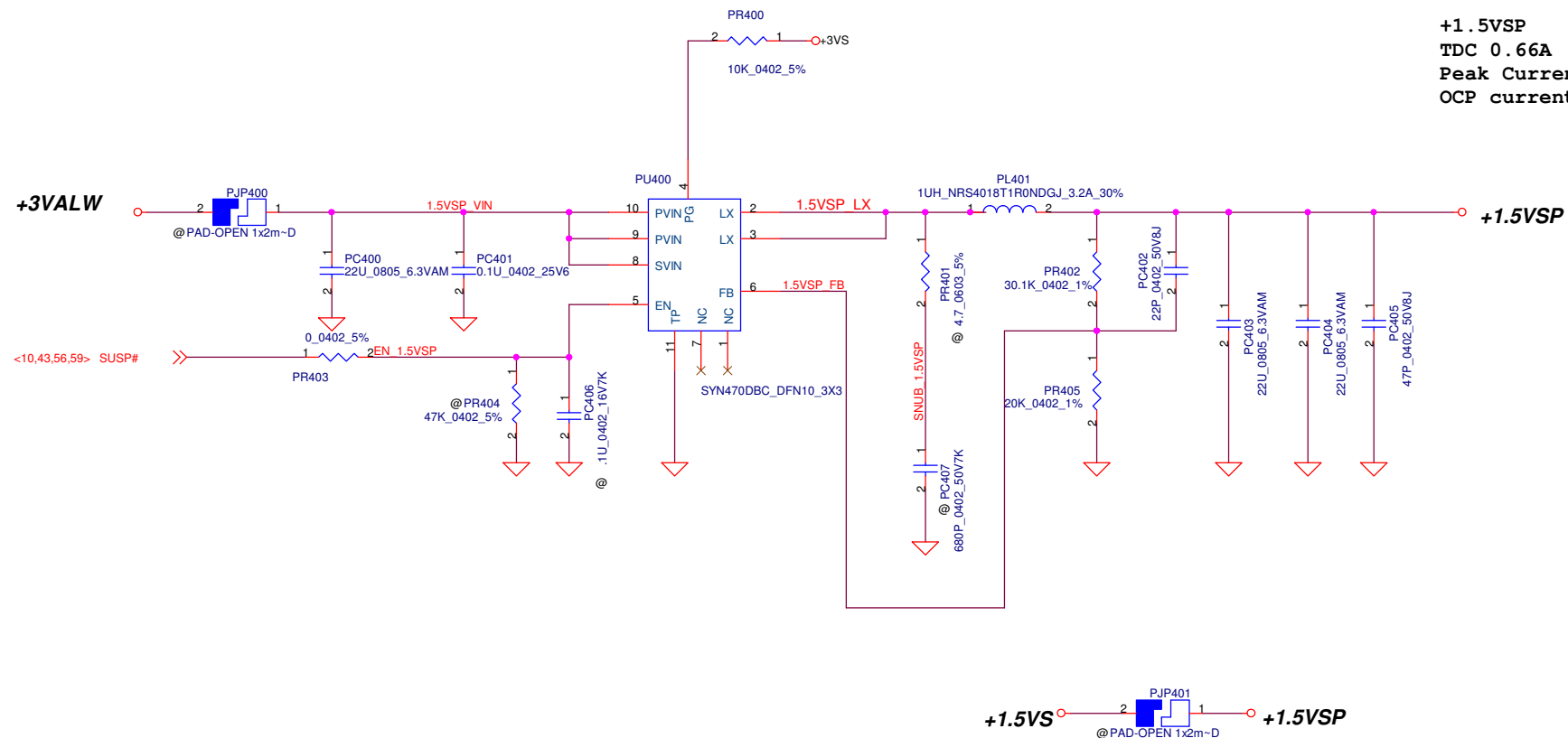
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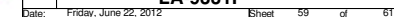


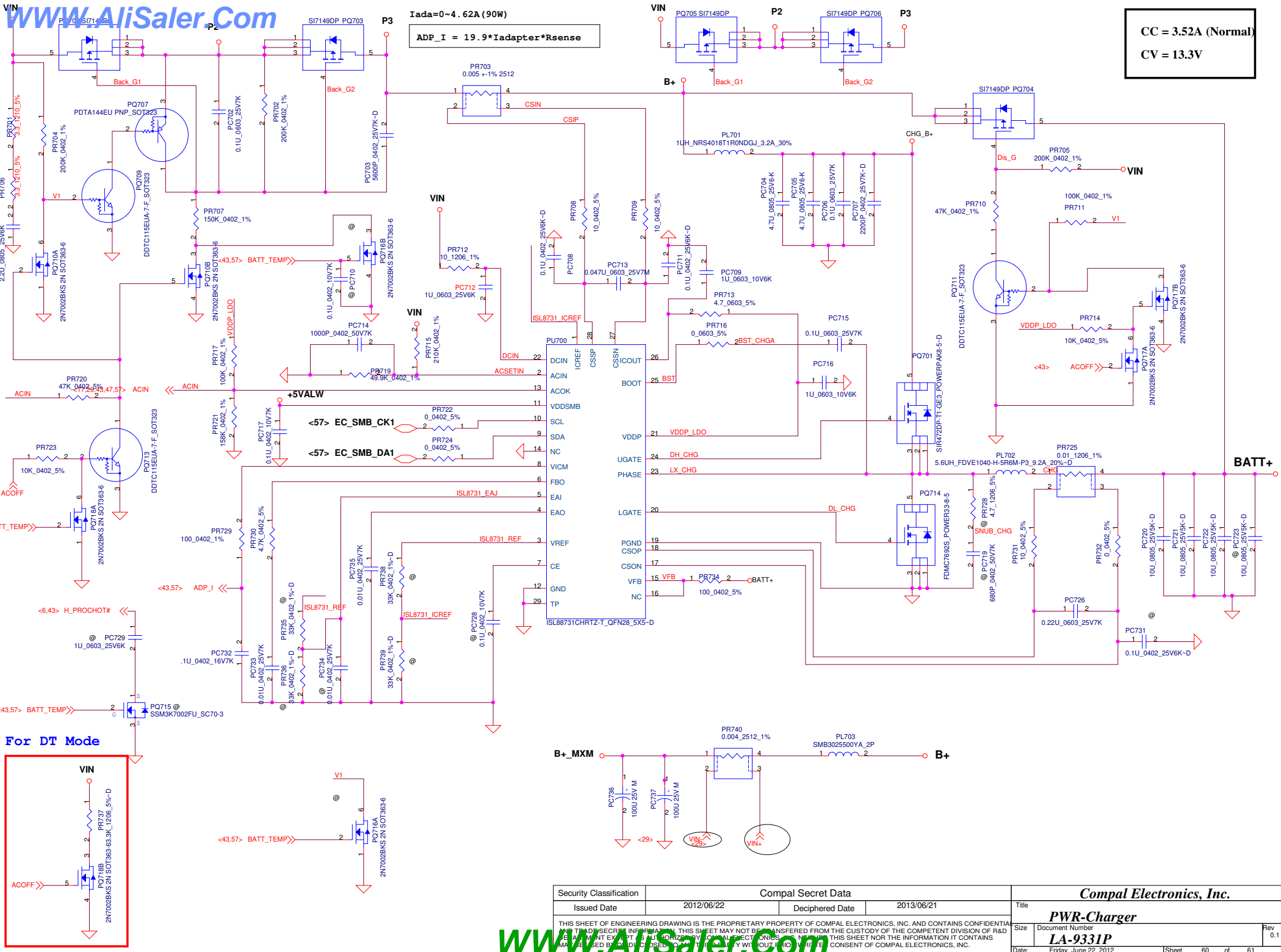
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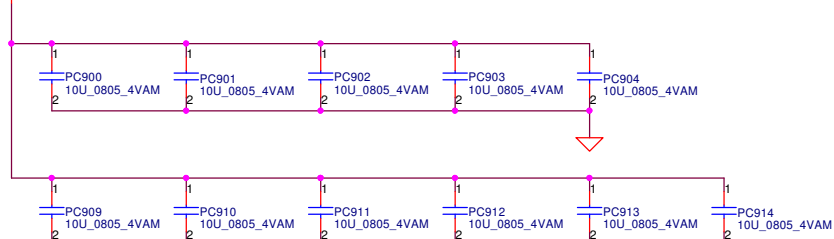
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Title		PWR-1.5VSP	
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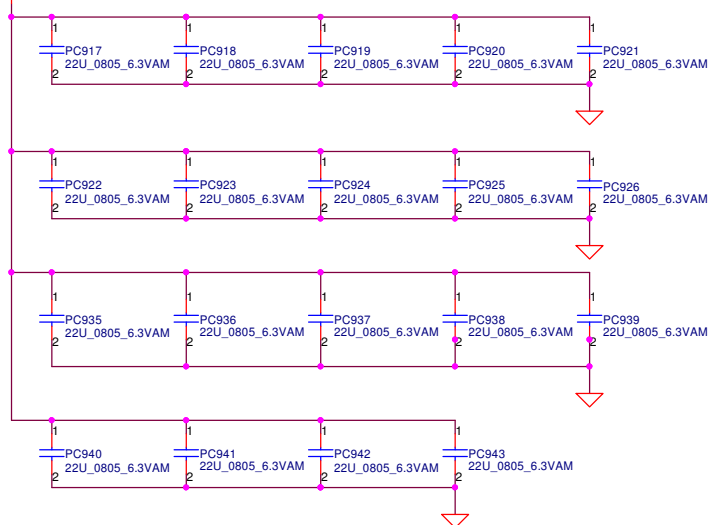




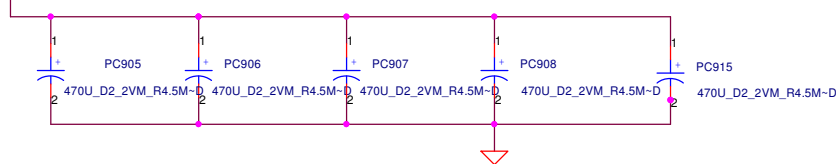
+VCC\_CORE



+VCC\_CORE



+VCC\_CORE



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Compal Electronics, Inc.

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